

# Compal Confidential

## C560 LA-A061P Schematics Document

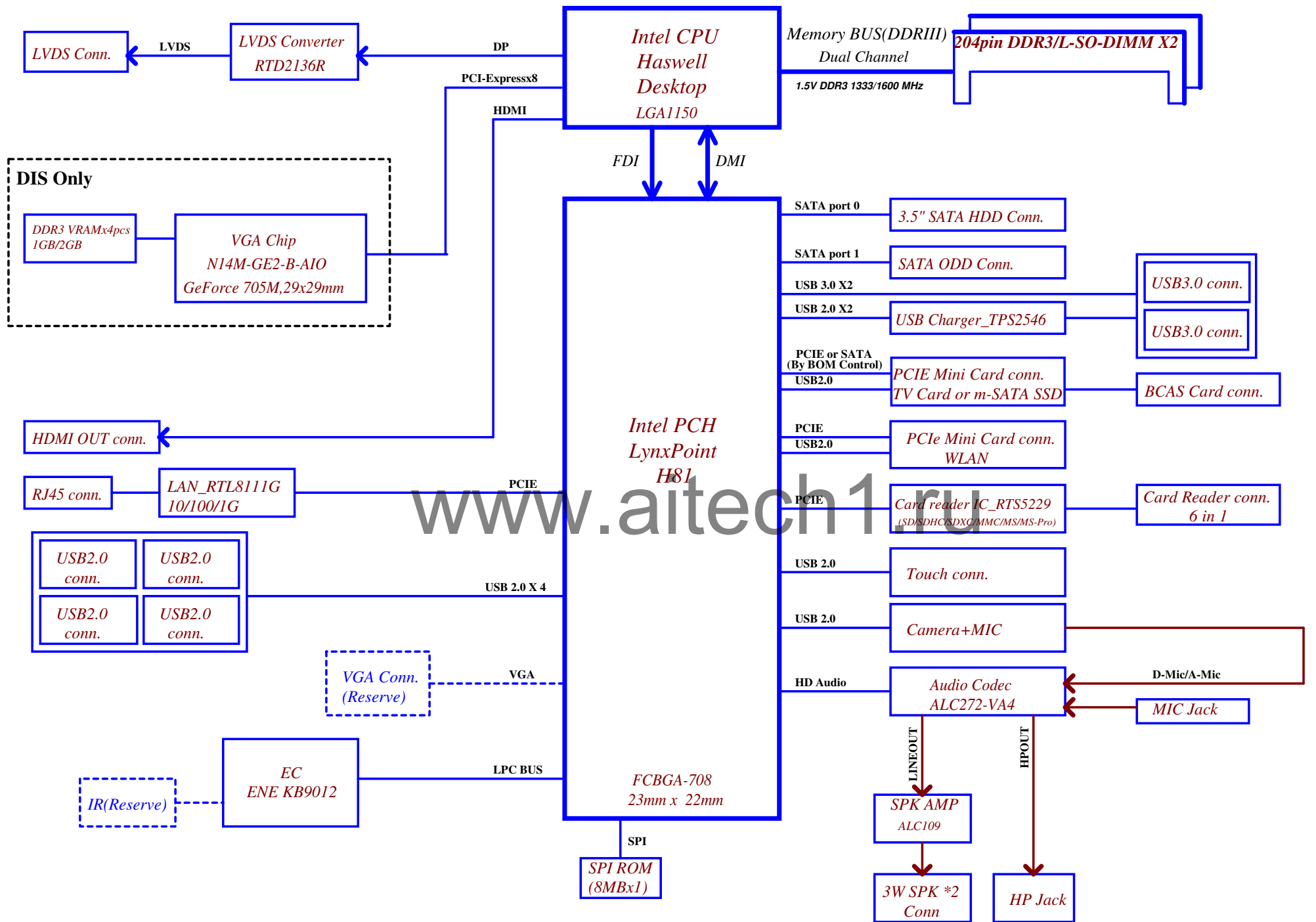
INTEL Haswell CPU with DDRIII + PCH Lynx-Point

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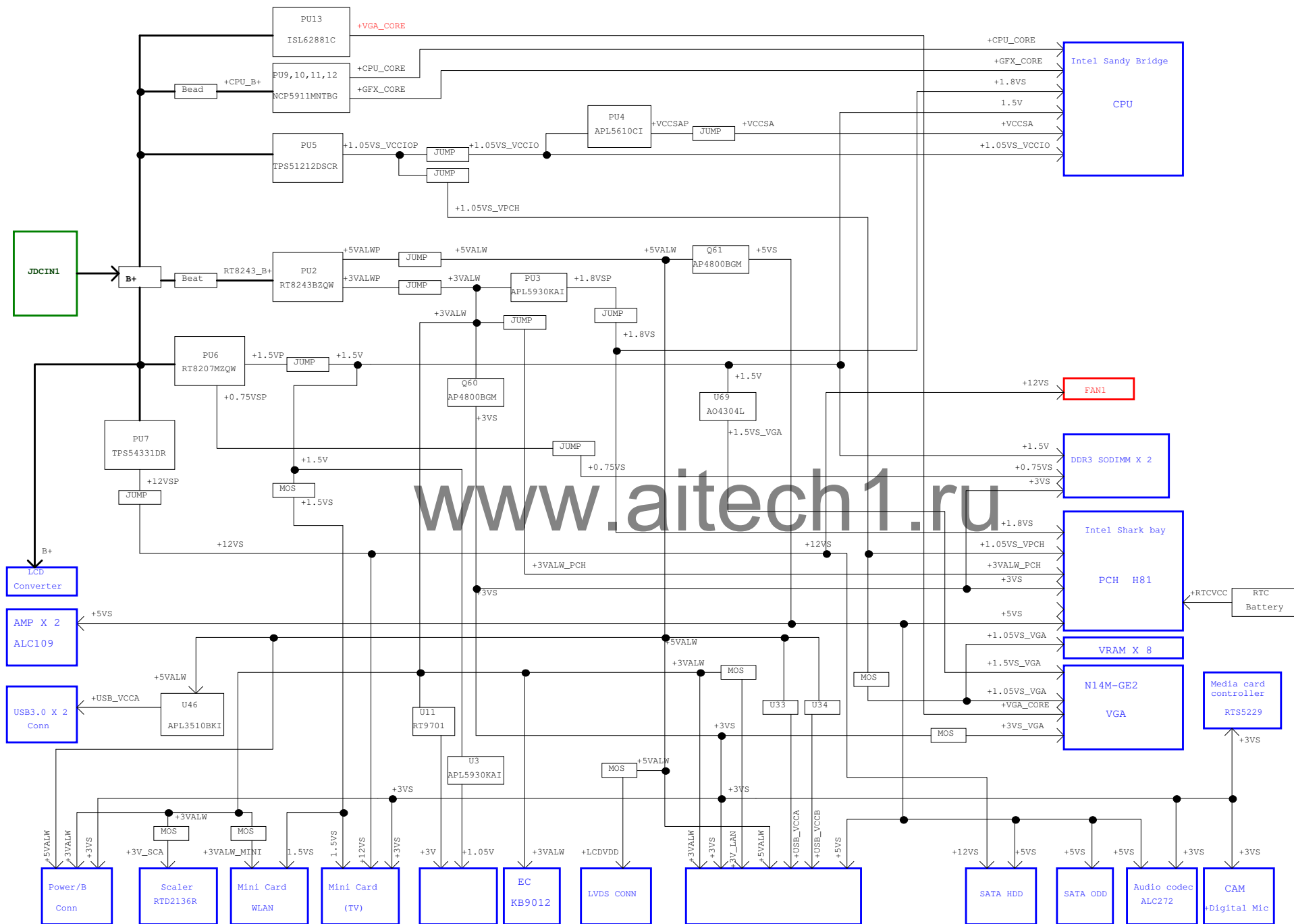
September 24, 2013

REV:1.0

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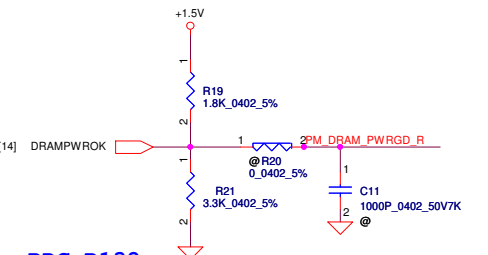
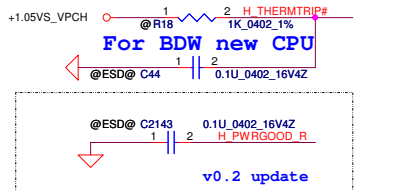
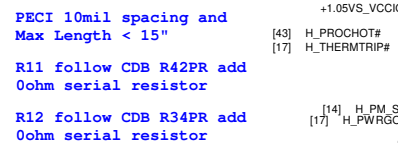


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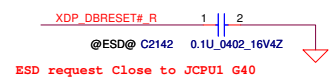
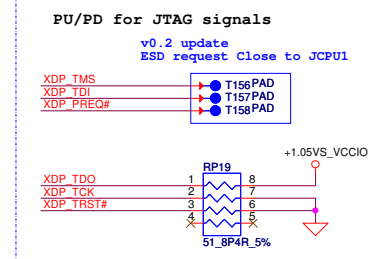
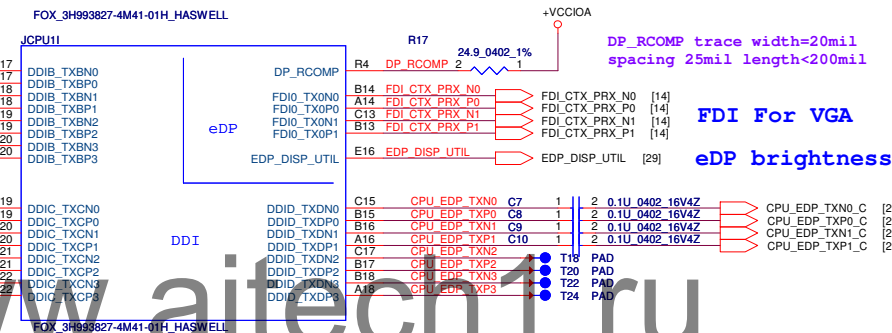
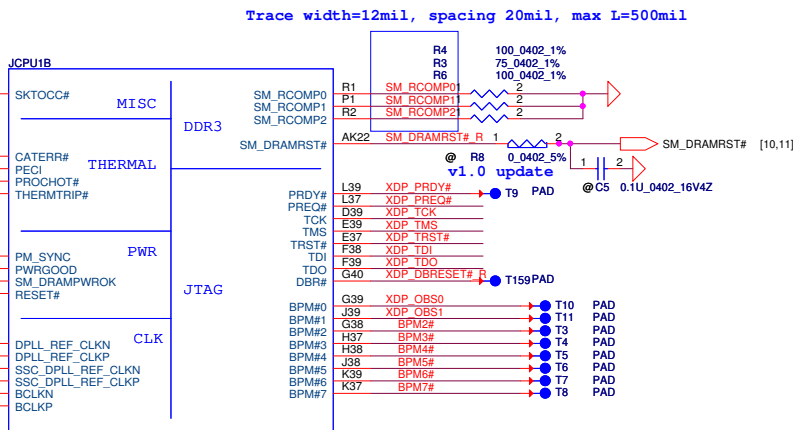








PDG P132   
HSW A0+LPT A0 change R21 to 4.7K, R19 to 3.3K



eDP  
(To LVDS Converter)

	Digital Display Interface (Differential Pairs)	HDMI Signals	Processor Digital Display Interface Pins
Port B	DDIO_T0_R0N0	HDMI_TX2_DP	DDIO_T0R0[0]
	DDIO_T0_R0P0	HDMI_TX2_DN	DDIO_T0R0[1]
	DDIO_T0_R1N0	HDMI_TX1_DP	DDIO_T0R1[0]
	DDIO_T0_R1P0	HDMI_TX1_DN	DDIO_T0R1[1]
	DDIO_T0_R2N0	HDMI_TX0_DP	DDIO_T0R2[0]
	DDIO_T0_R2P0	HDMI_TX0_DN	DDIO_T0R2[1]
	DDIO_T0_R3N0	HDMI_TX3_DP	DDIO_T0R3[0]
	DDIO_T0_R3P0	HDMI_TX3_DN	DDIO_T0R3[1]
	DDIO_T0_R4N0	HDMI_TX4_DP	DDIO_T0R4[0]
	DDIO_T0_R4P0	HDMI_TX4_DN	DDIO_T0R4[1]
Port C	DDIO_T0_R5N0	HDMI_TX5_DP	DDIO_T0R5[0]
	DDIO_T0_R5P0	HDMI_TX5_DN	DDIO_T0R5[1]
	DDIO_T0_R6N0	HDMI_TX6_DP	DDIO_T0R6[0]
	DDIO_T0_R6P0	HDMI_TX6_DN	DDIO_T0R6[1]
	DDIO_T0_R7N0	HDMI_TX7_DP	DDIO_T0R7[0]
Port D	DDIO_T0_R8N0	HDMI_TX8_DP	DDIO_T0R8[0]
	DDIO_T0_R8P0	HDMI_TX8_DN	DDIO_T0R8[1]
	DDIO_T0_R9N0	HDMI_TX9_DP	DDIO_T0R9[0]
	DDIO_T0_R9P0	HDMI_TX9_DN	DDIO_T0R9[1]
	DDIO_T0_R10N0	HDMI_TX10_DP	DDIO_T0R10[0]

v0.2 update

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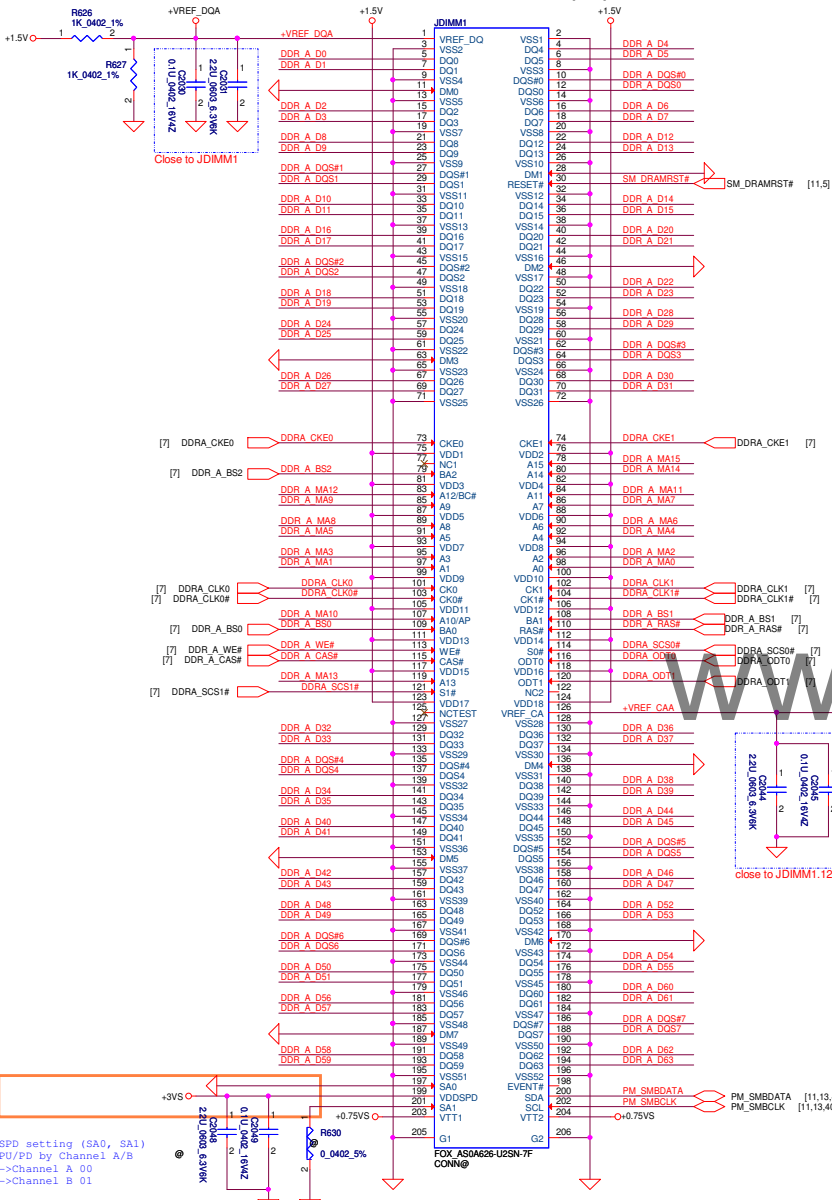








# CHA SO-DIMM Q(A0)



Standard H:5.2mm

Layout Note:  
Place near JDIMM1

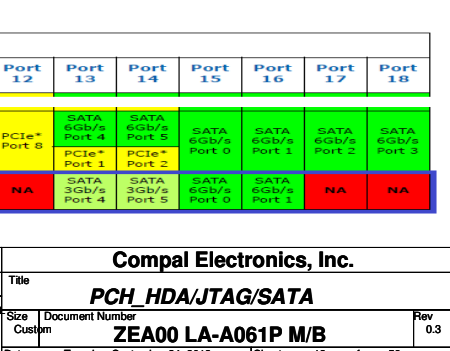
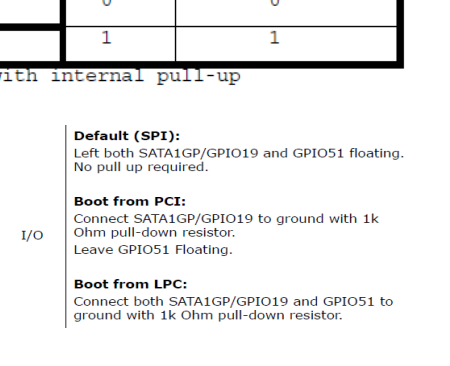
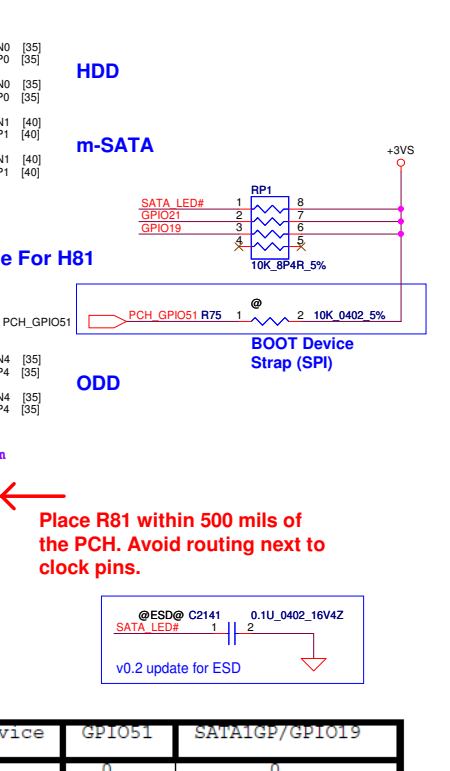
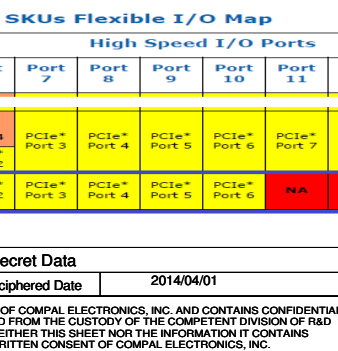
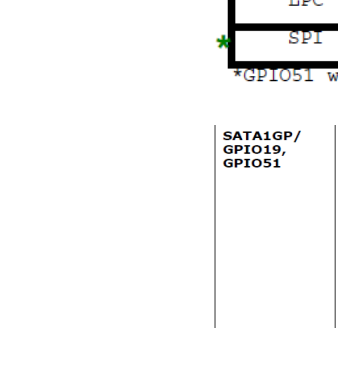
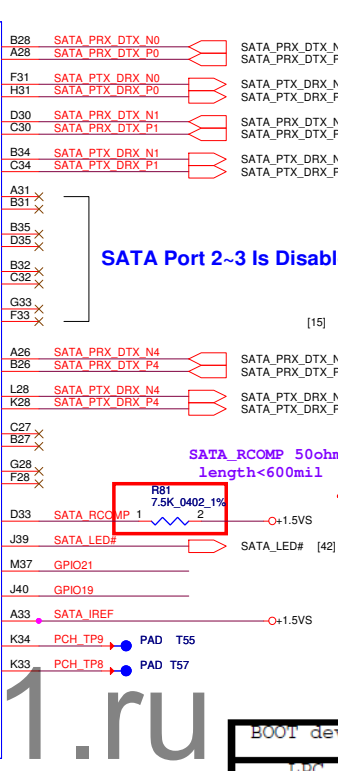
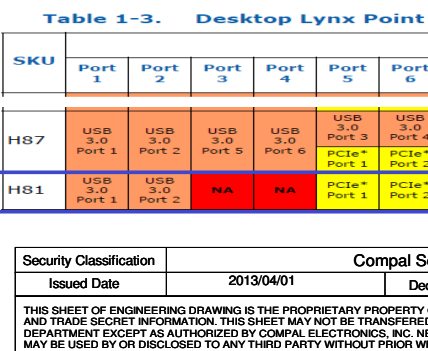
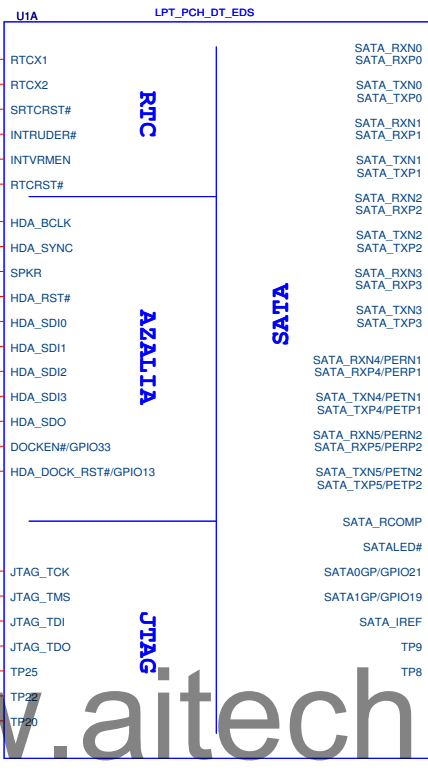
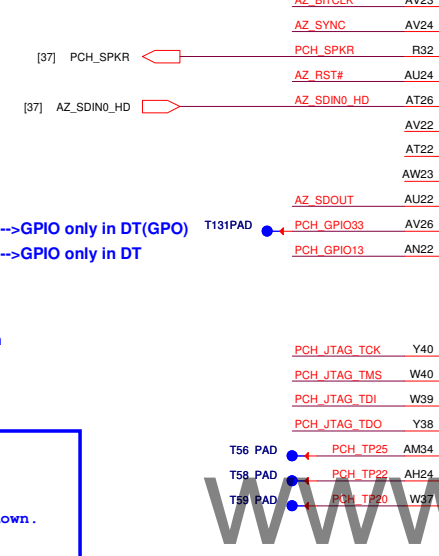
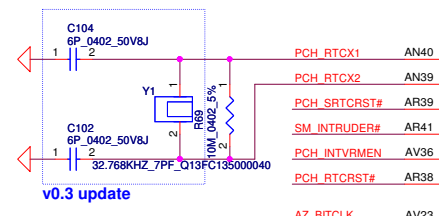
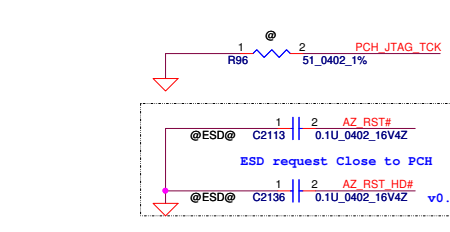
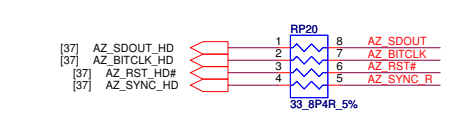
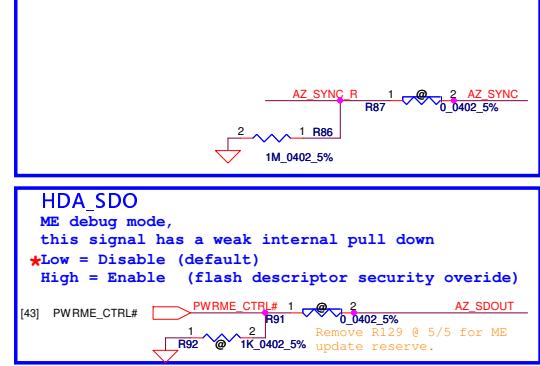
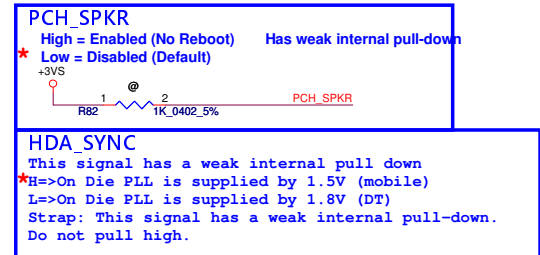
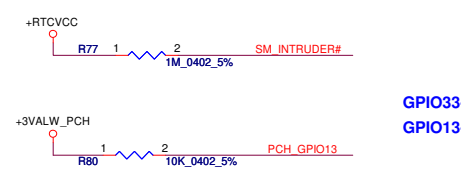
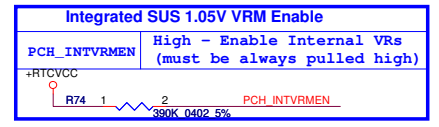
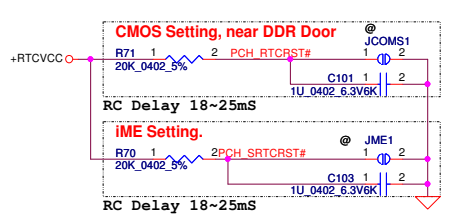
Layout Note: Place these Caps near  
+1.5V of JDIMM1

Layout Note:  
Place near JDIMM1 Pin203 and 204

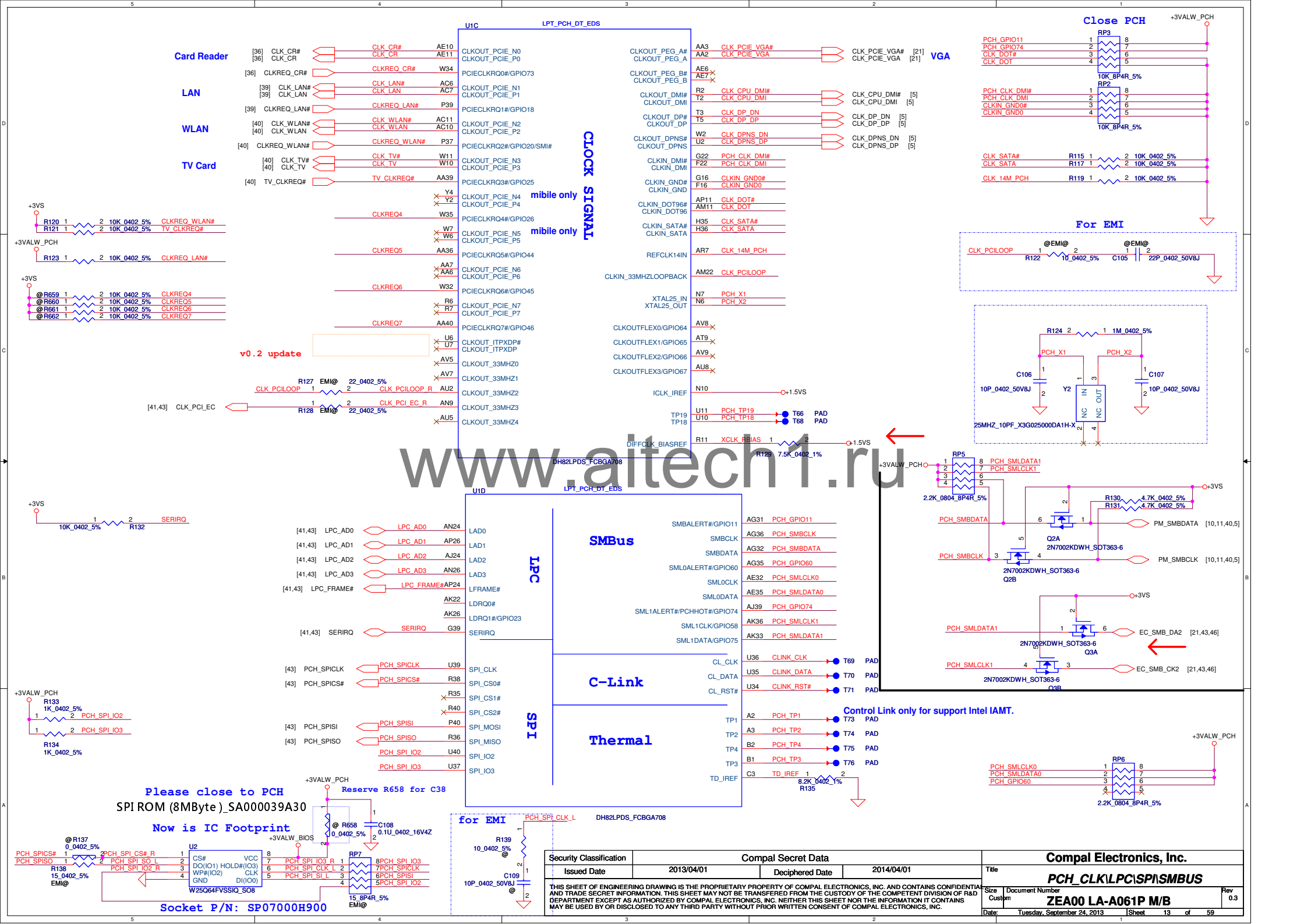
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				DDRIII-SODIMMA	
				ZEA00 LA-A061P M/B	
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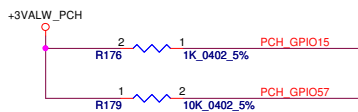








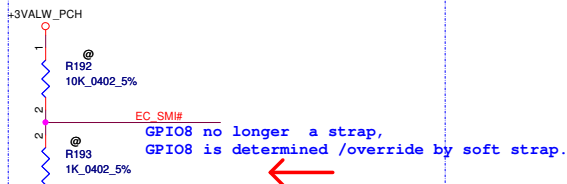




#### GPIO8

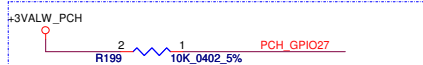
Integrated Clock Chip Enable (Removed)

H: Disable  
L: Enable



This signal has a weak internal pull-up but requires an external pull down.

The current default is clock enable



In Deep Sleep Power Well. Unmuxed. Defaults to GPI. Not used Weak pull-up 10kΩ to VccDSW3\_3 -->Check list1.5 P402. PD to GND for Huron River!!

#### GPIO28

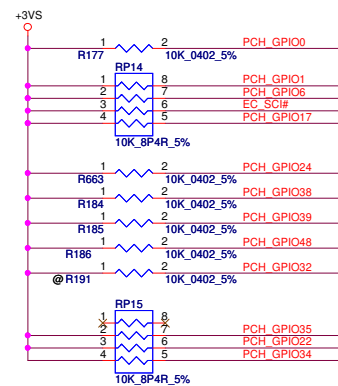
On-Die PLL Voltage Regulator

H: Enable  
L: Disable



Clock validation strap  
ICG is EN when LOW  
\*GPIO36 with internal pull-down

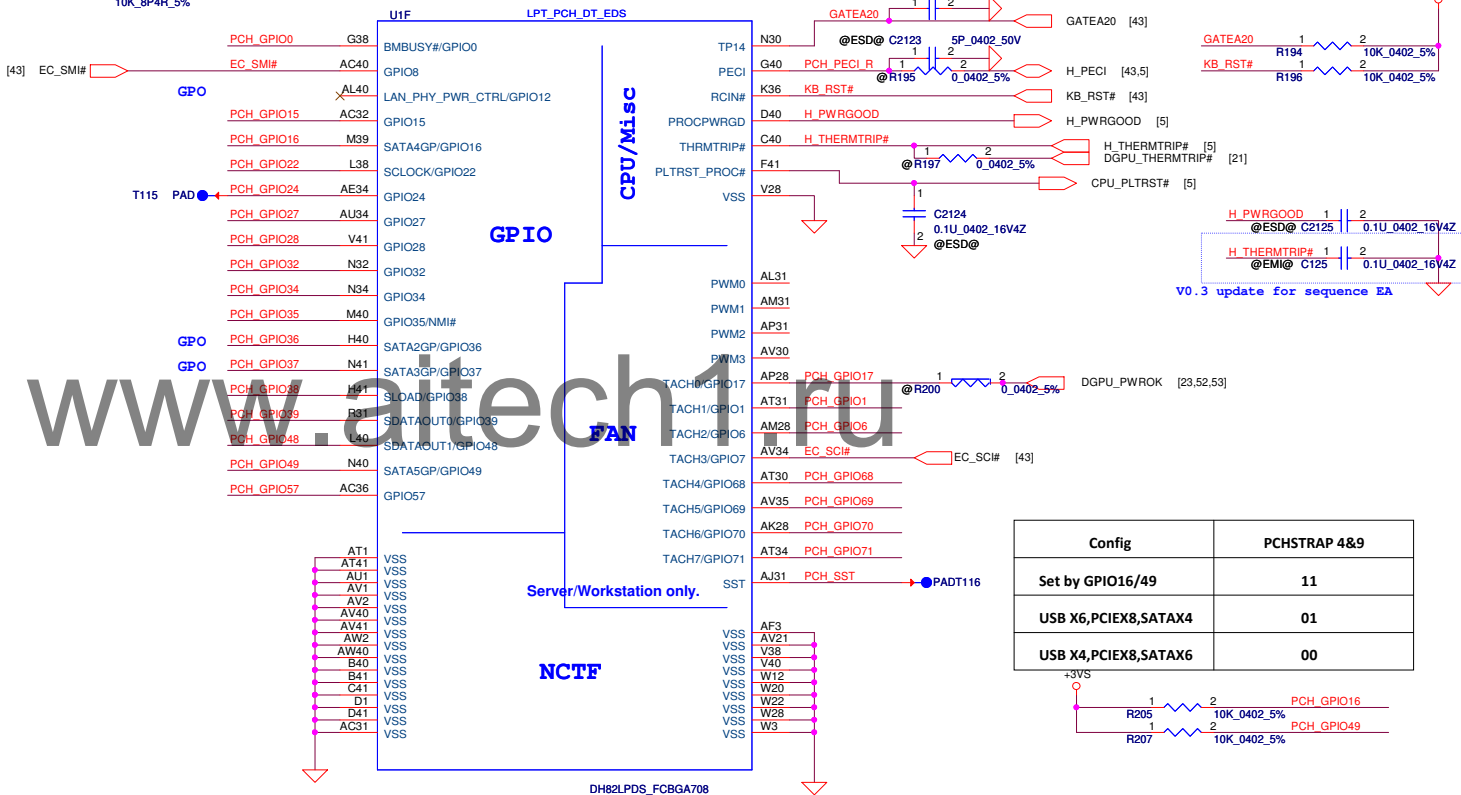
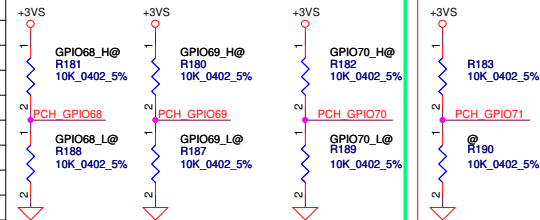
TL5  
Hi:with confidentiality  
Low:with no confidentiality  
\*GPIO37 with internal pull-down



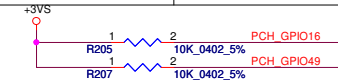
120821

SKU ID	GPIO68	GPIO69	GPIO69
SKU1	0	0	0
SKU2	0	0	1
SKU3	0	1	0
SKU4	0	1	1
SKU5	1	0	0
SKU6	1	0	1
SKU7	1	1	0
SKU8	1	1	1

#### SKU ID TABLE

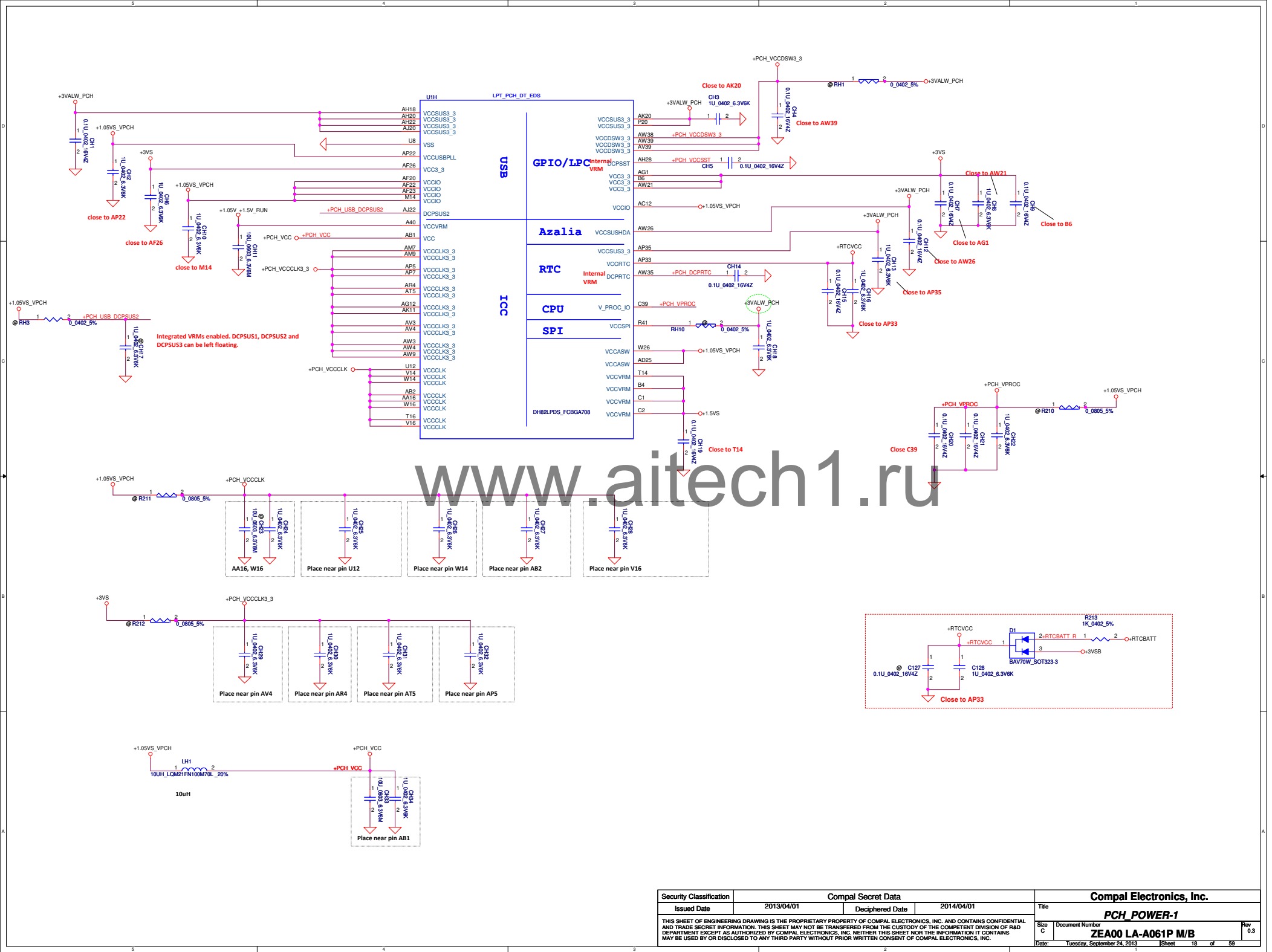


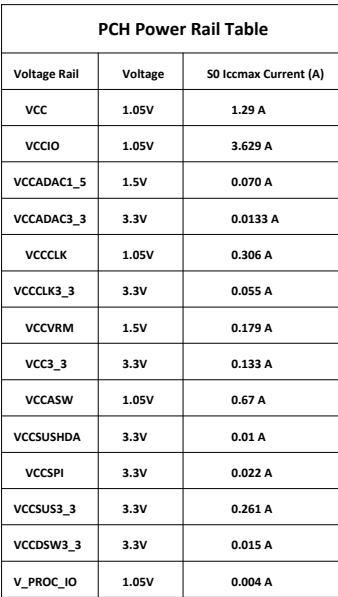
Config	PCHSTRAP 4&9
Set by GPIO16/49	11
USB X6,PCIEX8,SATAx4	01
USB X4,PCIEX8,SATAx6	00



Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)							(00)	(00)						
				USB3 3	USB3 4							PCIE 1	PCIE 2						
				(01)	(01)							(01)	(01)						

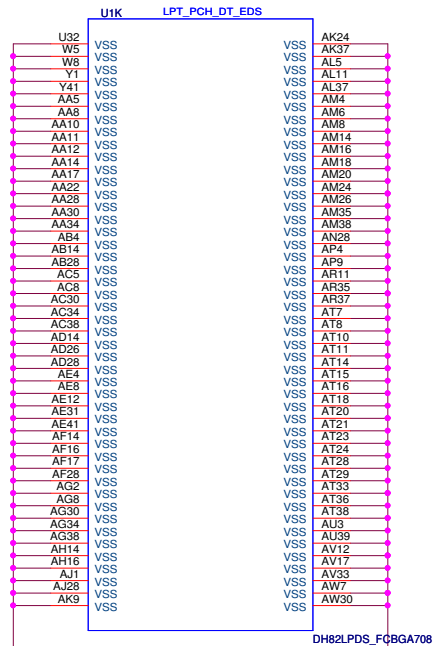
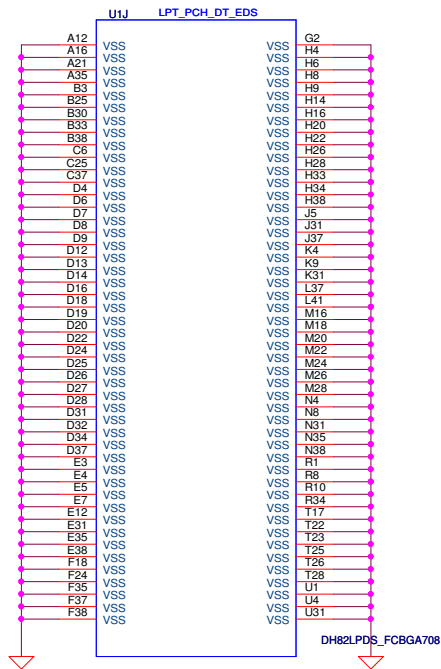
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PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

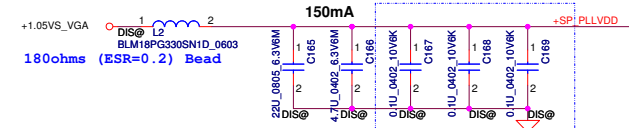
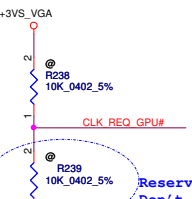
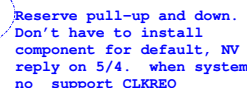
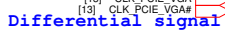
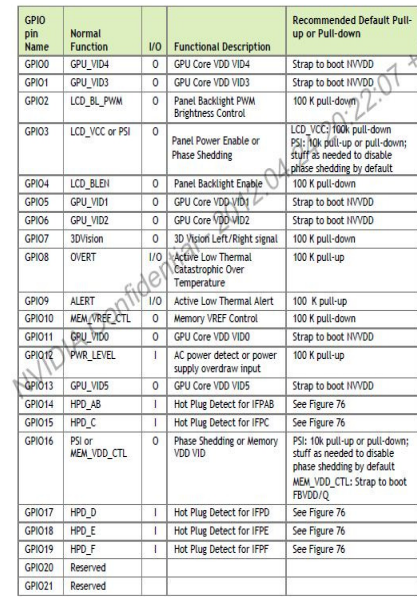
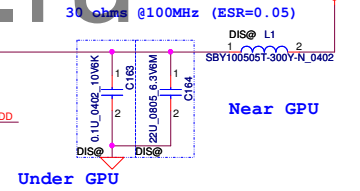
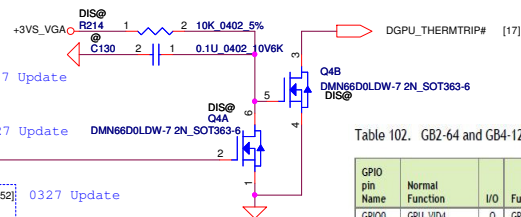




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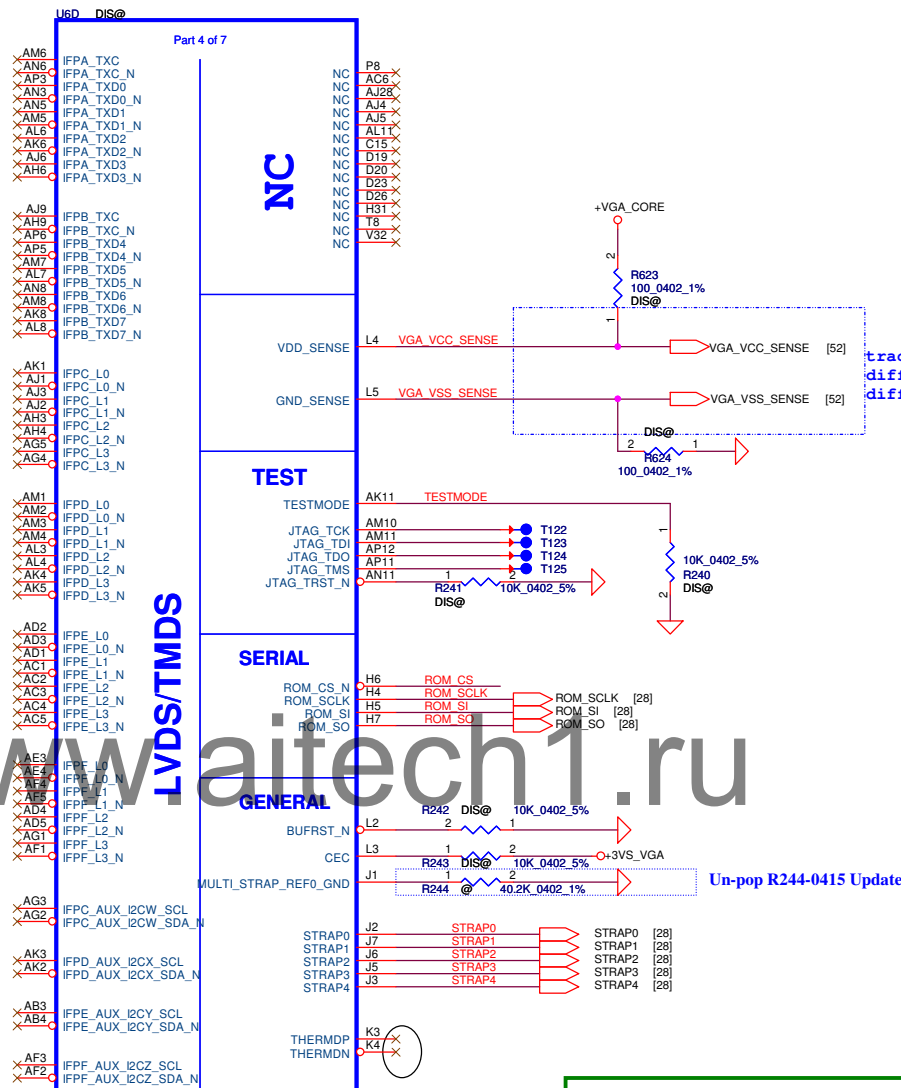




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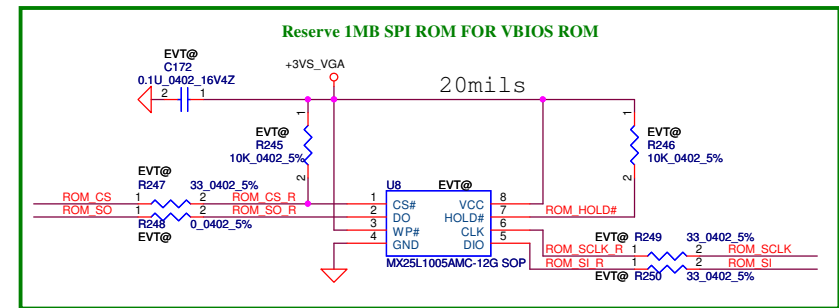
Table 66. N13x Family Display Link Summary

Link	Description
Link A	LVDS (Single Link or Dual Link with IFPB)
Link B	LVDS (Dual Link with IFPA)
Link C	DisplayPort, HDMI
Link D	DisplayPort, eDP
Link E	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI
Link F	DisplayPort, DVI (Dual Link with IFPE), HDMI

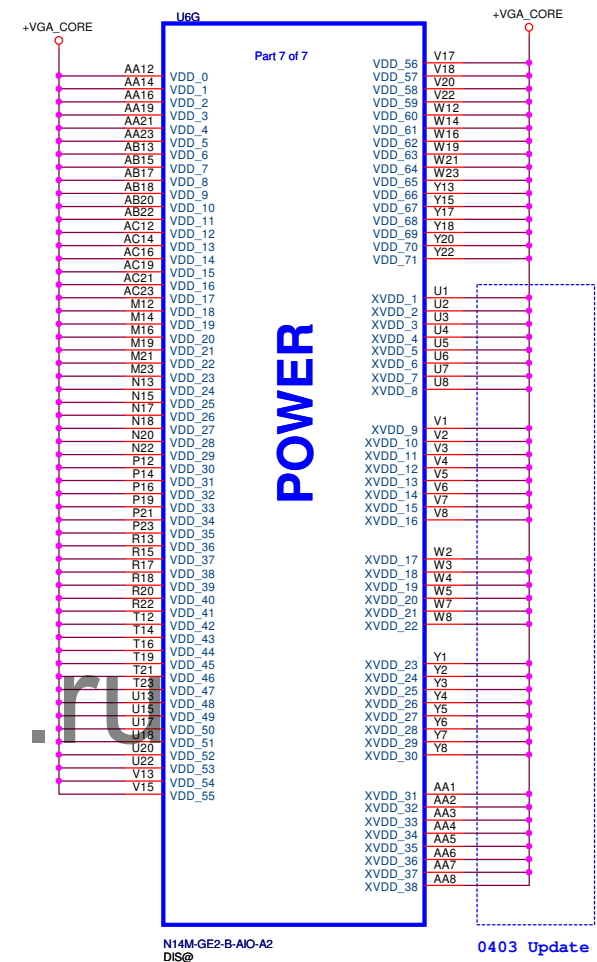
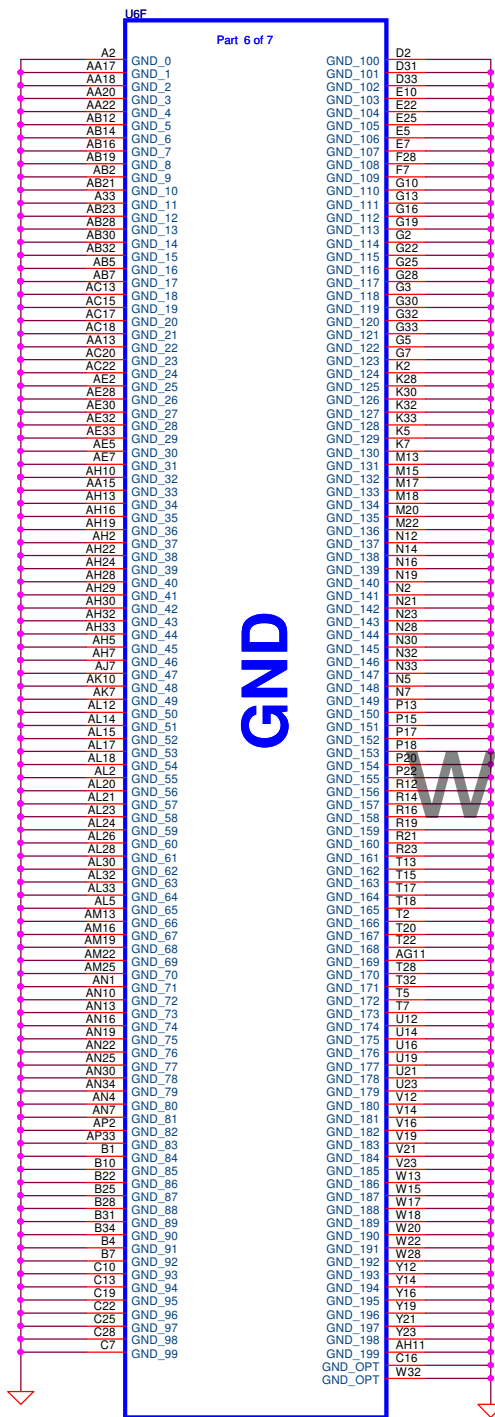


trace width: 16mils  
differential voltage sensing.  
differential signal routing.

Un-pop R244-0415 Update





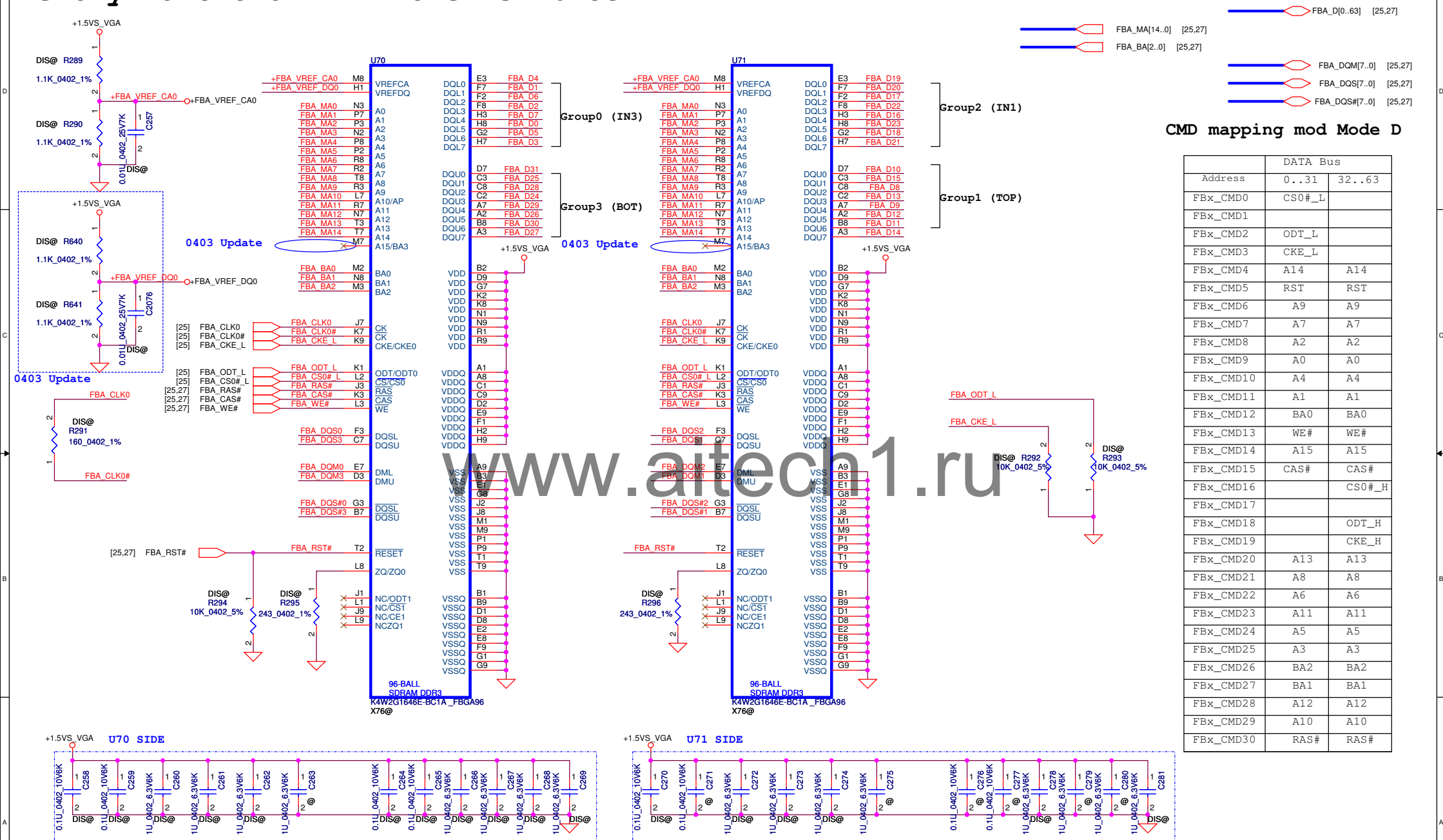


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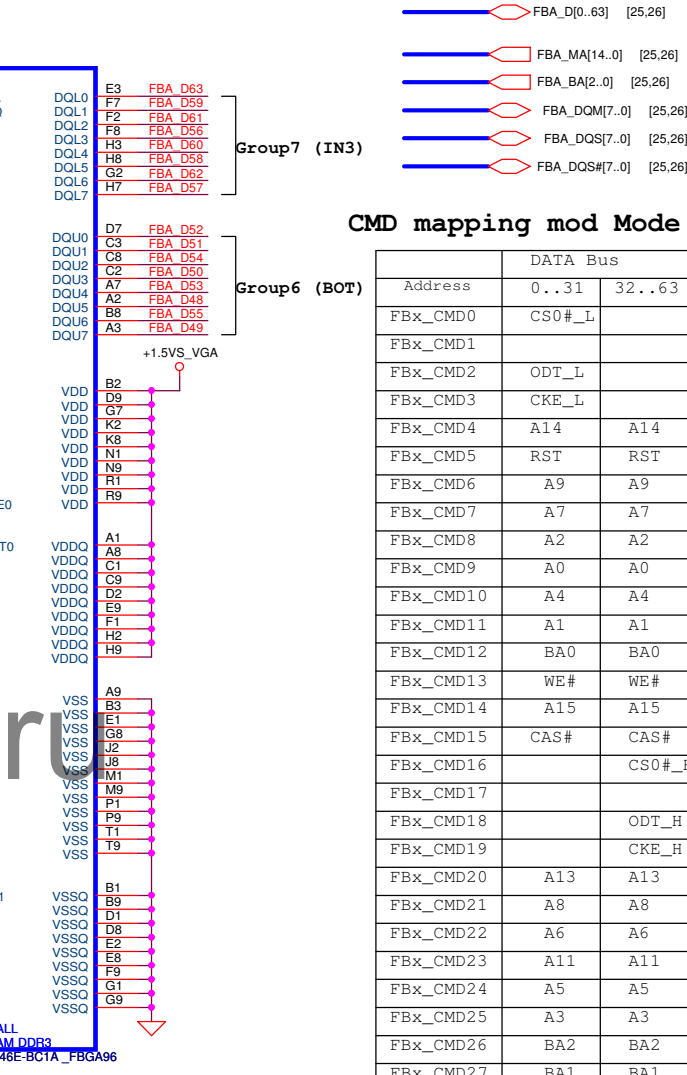
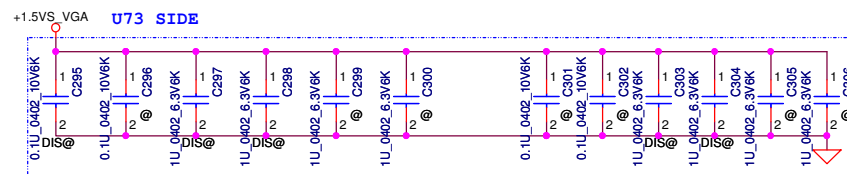
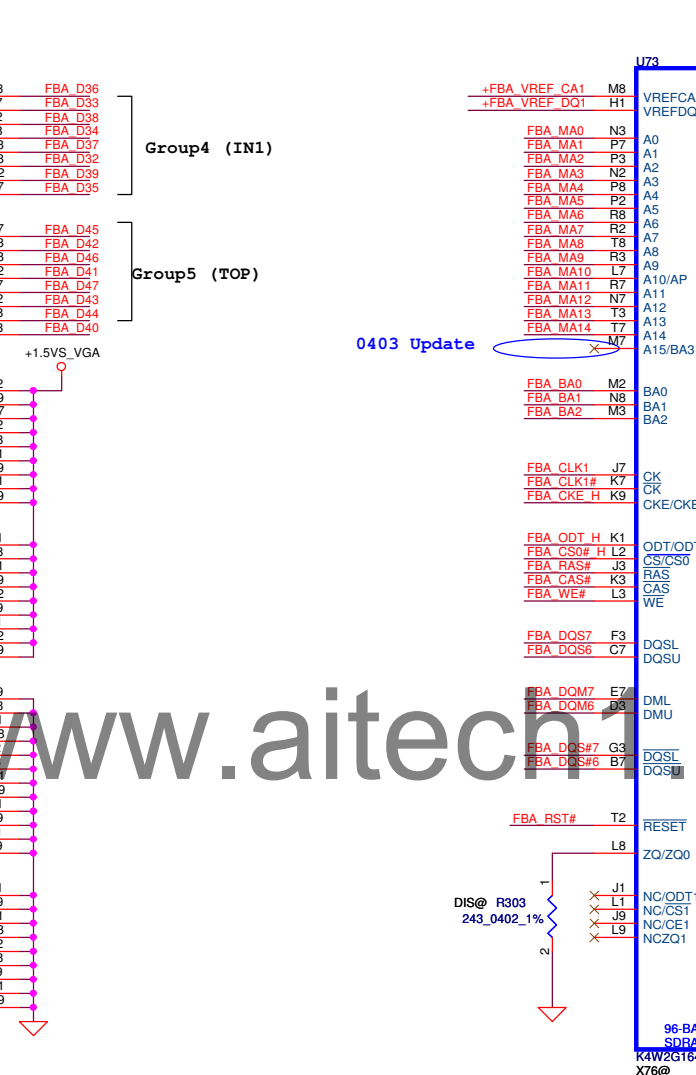
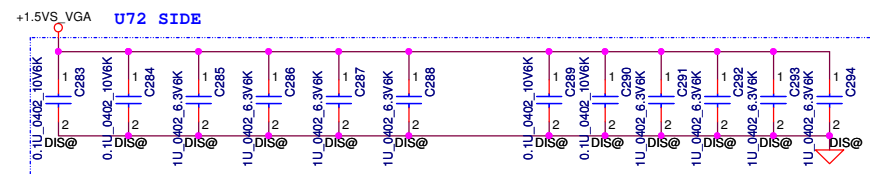
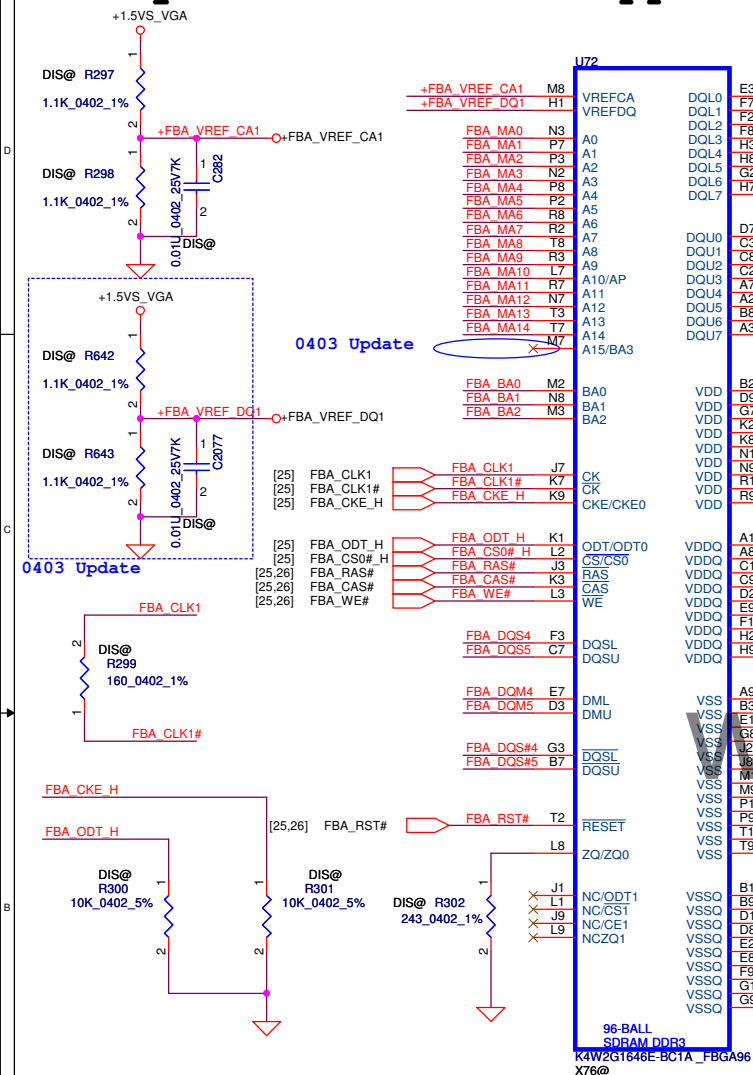
## Memory Partition A - Lower 32 bits



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

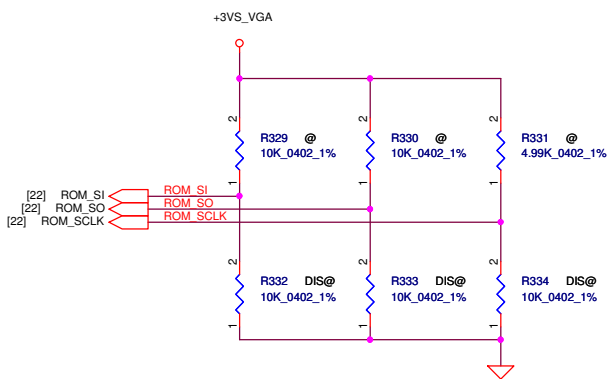
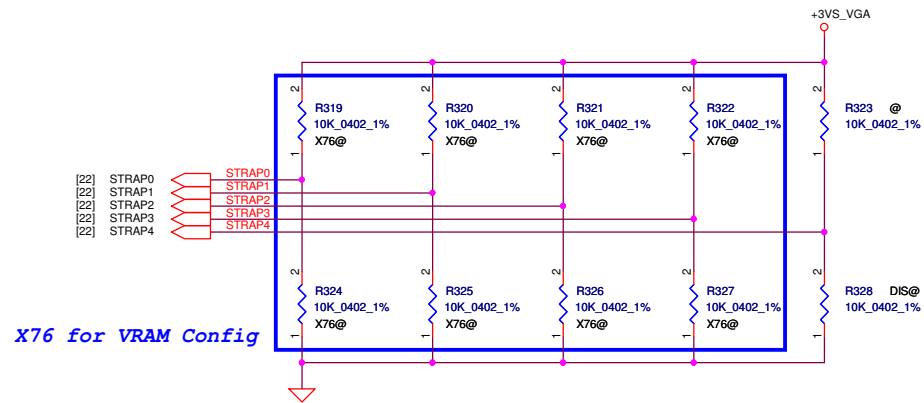
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2013/04/01	Deciphered Date	2014/04/01	Title	<b>N14M-GE2-VRAM A Lower</b>	
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## Memory Partition A - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_I
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



[PUN-06026-001]

Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k $\Omega$	Pull-down to GND
ROM_SI	SUB_VENDOR	10k $\Omega$	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k $\Omega$	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k $\Omega$	See Note
STRAP1	RAM_CFG[1]	10k $\Omega$	See Note
STRAP2	RAM_CFG[2]	10k $\Omega$	See Note
STRAP3	RAM_CFG[3]	10k $\Omega$	See Note
STRAP4	PCIE_MAX_SPEED	10k $\Omega$	Pull-down to GND

[VRAM Config-RVL-06366-001]

GPU	Frenq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0
N14M-GE2	900 MHz	128M* 16* 4 1GB	Hynix (0x6) H5TQ2G63BFR-11C SA00003YO10	0 R327 PD 10K	1 R321 PU 10K	1 R320 PU 10K	0 R324 PD 10K
			Samsung (0x5) K4W2G1646E-BC11 SA00005SH00	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Micron (0x1) MT41J128M16JT-107G:K SA00005SM30	0 R327 PD 10K	0 R326 PD 10K	0 R325 PD 10K	1 R319 PU 10K
N14M-GE2	900 MHz	256M* 16* 4 2GB	Micron (0xD) MT41K256M16HA-107G:E SA00006SD20	1 R322 PU 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Samsung (0xB) K4W4G1646B-HC11 SA000068R10	1 R322 PU 10K	0 R326 PD 10K	1 R320 PU 10K	1 R319 PU 10K
			Hynix (0x4) H5TC4G63AFR-11C SA00006E800	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	0 R324 PD 10K

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						Size		Document Number		Rev	
								ZEA00 LA-A061P M/B		0.3	
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## Power Consumption:

Pin 22 (PVCC) < 50 mA

Pin 18 (SWR\_VDD) < 200mA (layout trace > 40 mil)

Pin5 (DPV33) < 20mA

Pin 17 (SWR\_LX) < 600mA (layout trace > 60 mil)

Pin 15 (SWR\_VCCK) < 100mA (layout trace > 60 mil)

Pin 43 (VCCK) < 50mA

Pin 11 (DPV12) < 100mA

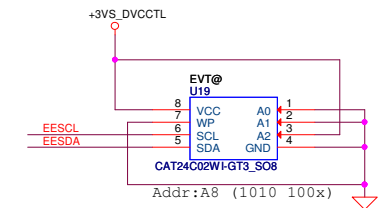
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S CER CAP .1U 16V Z Y5V 0402

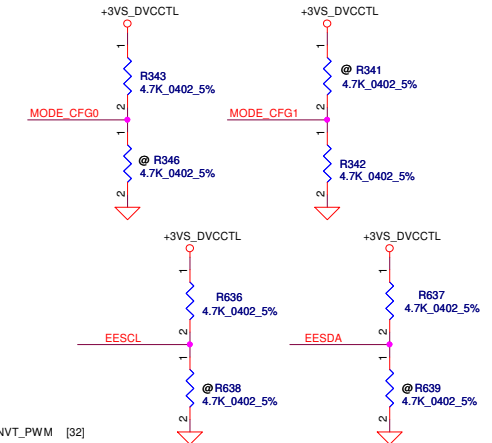
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v0.2 update

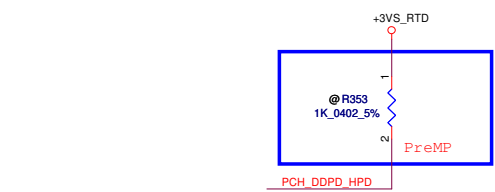
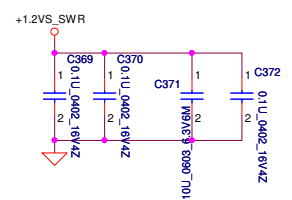
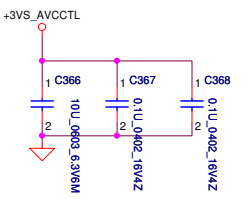
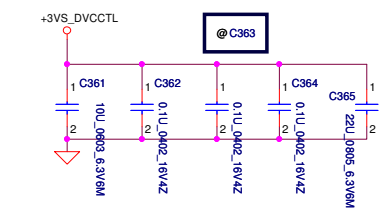
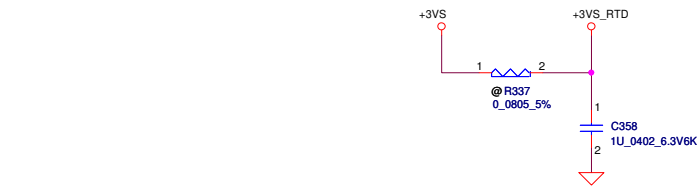
## Vendor suggest to reserve for FW/EDID debug



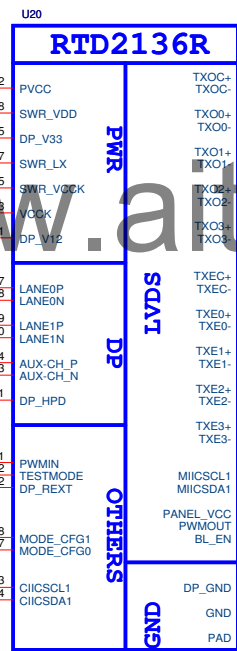
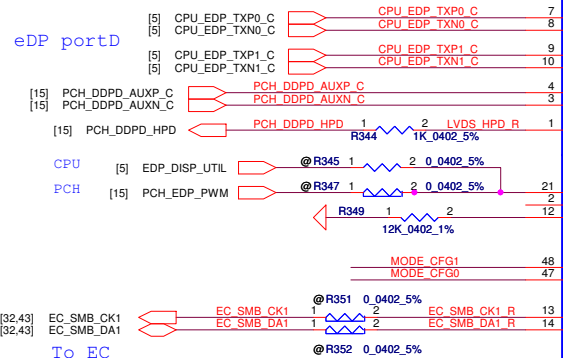
EVT Debug Only, un-pop for DVT



Pin 47			
	0	1	
Pin 48	0	X	EP Mode
	1	ROM	EEPROM



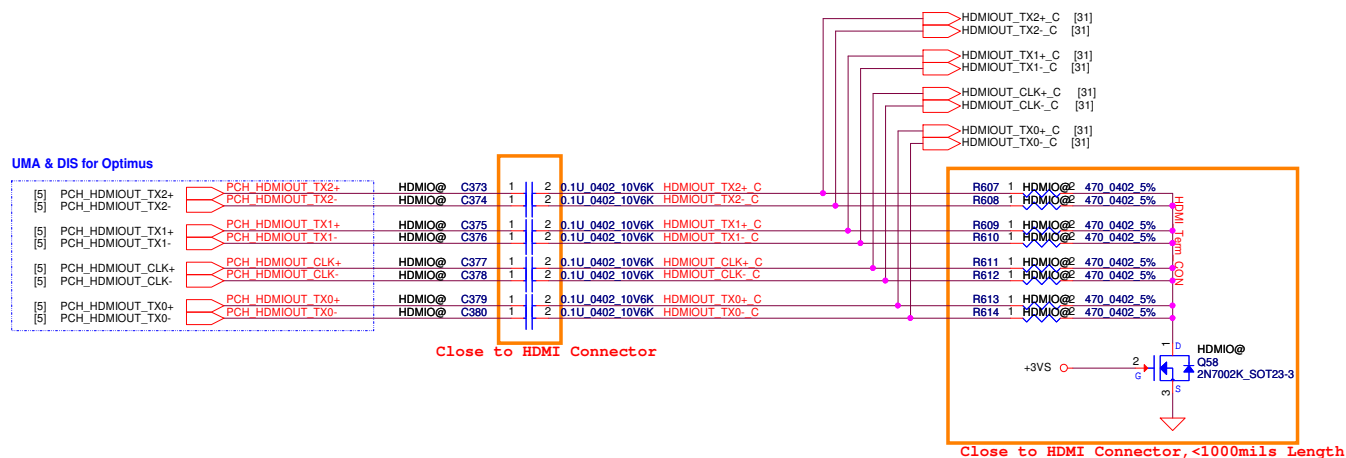
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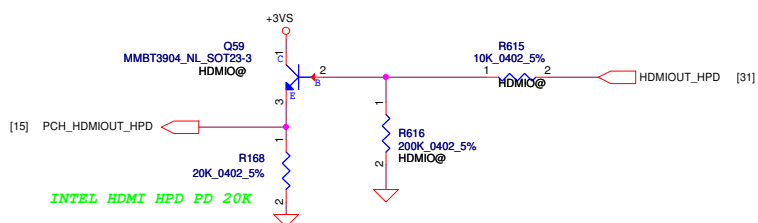
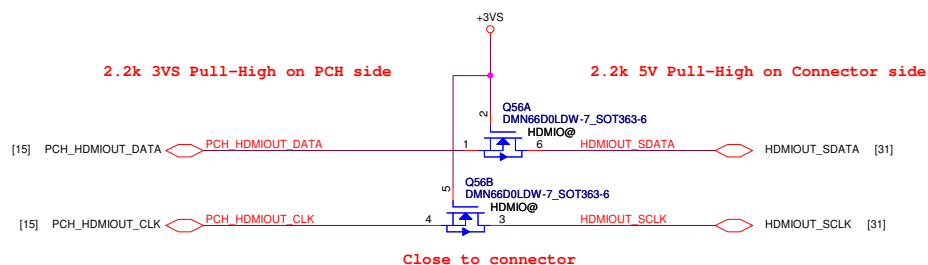
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UMA & DIS for Optimus

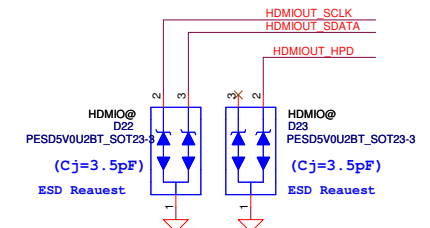
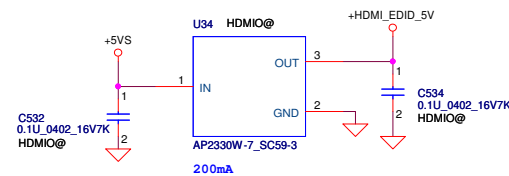
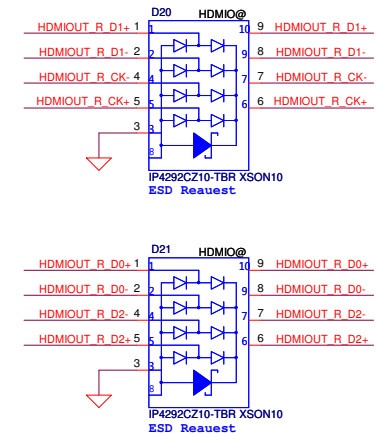
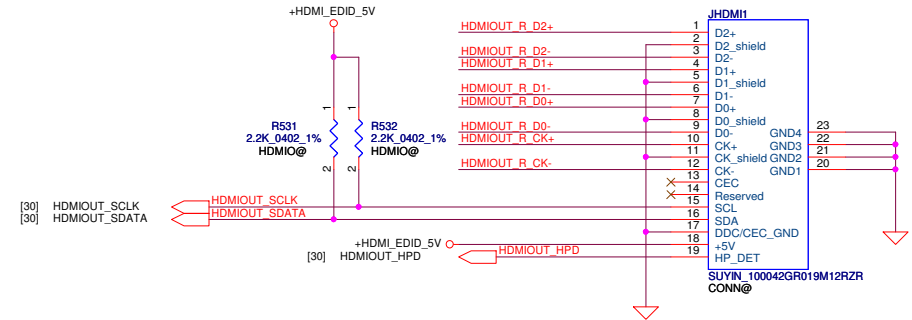
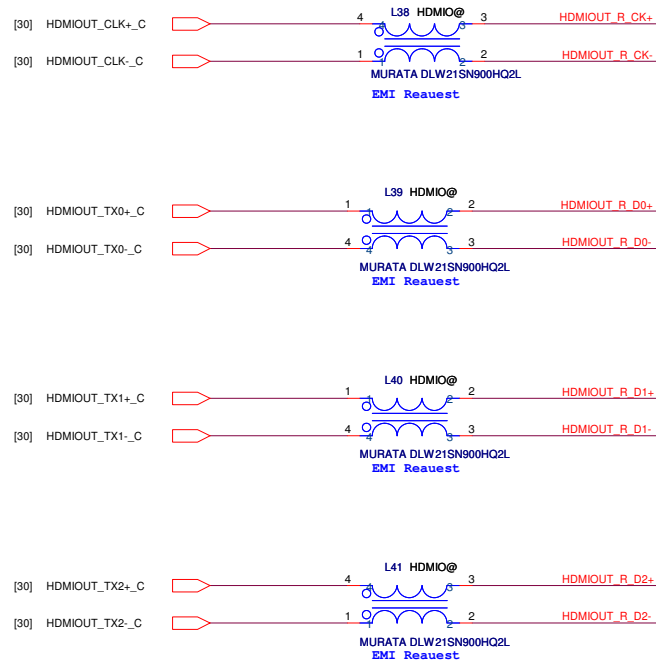


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Size	Custom	Document Number	ZEA00 LA-A061P M/B		Rev
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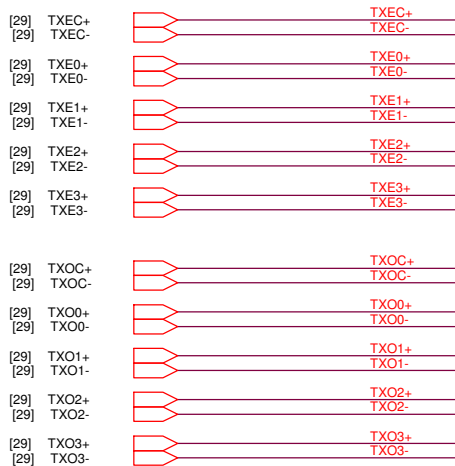
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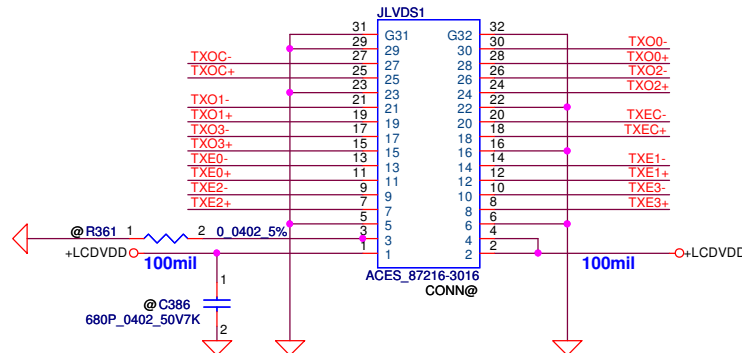
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EMI Request

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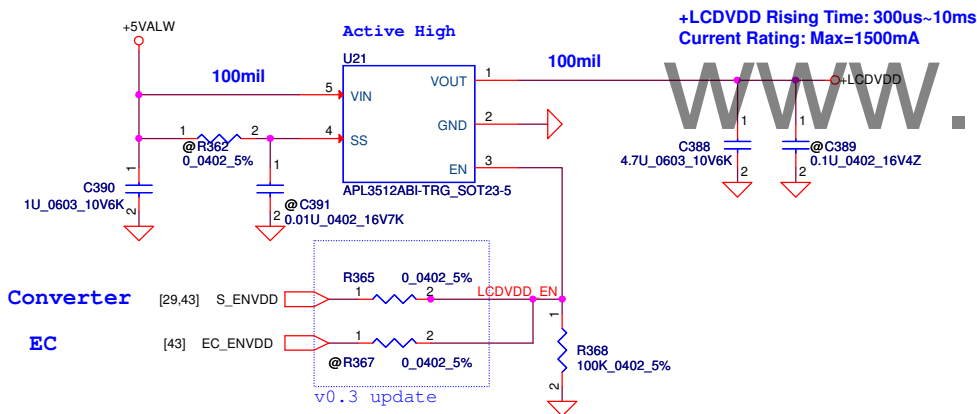
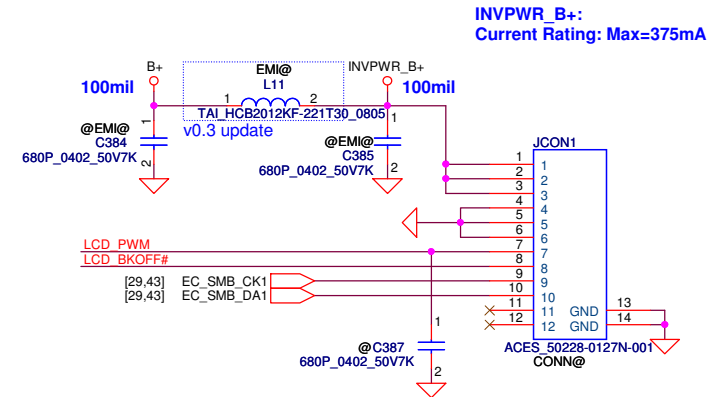
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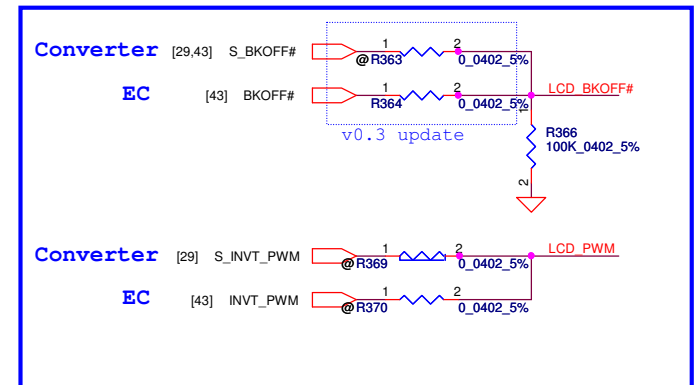
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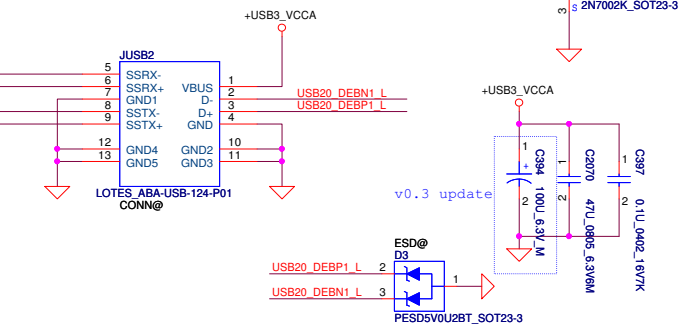
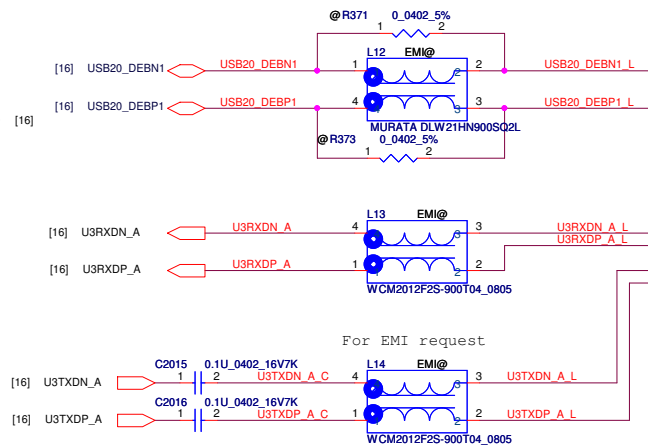
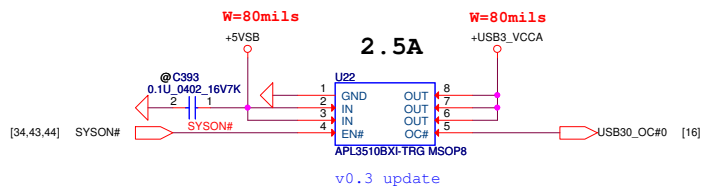
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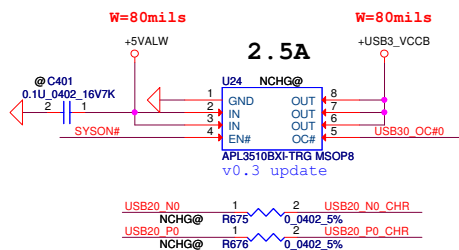
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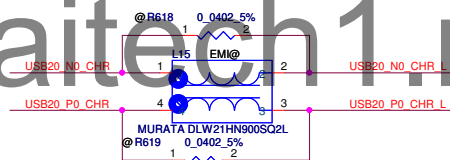
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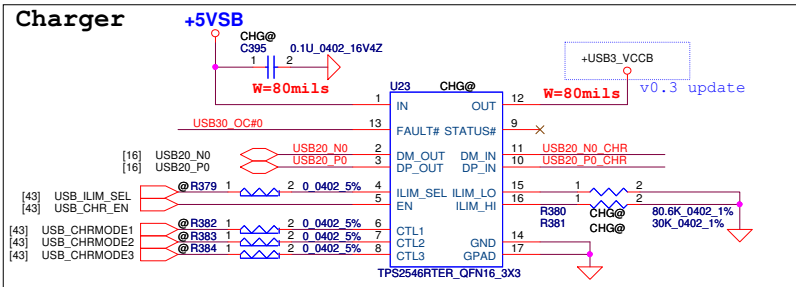
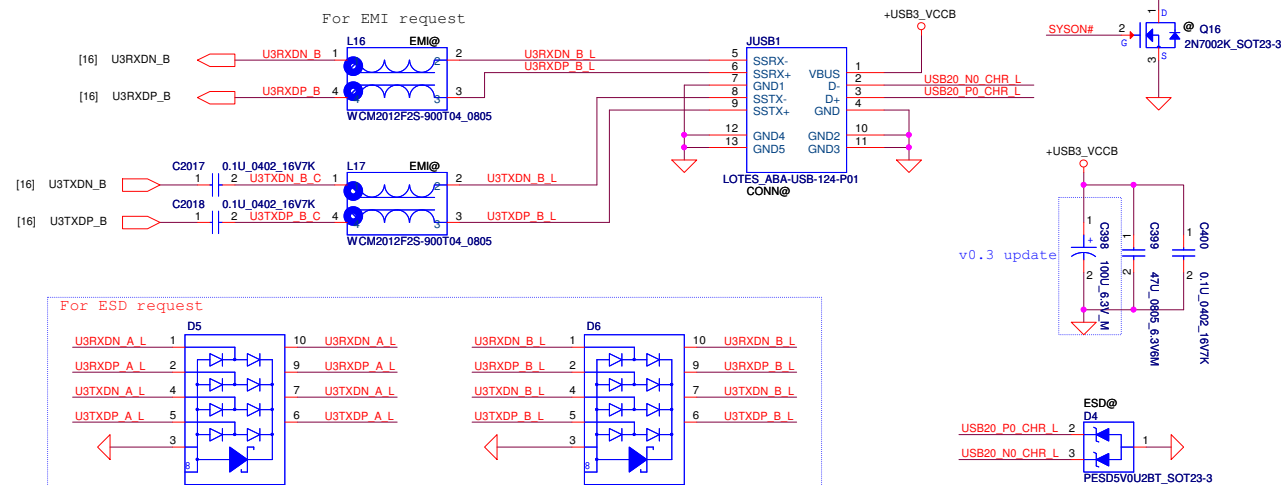
## Non Changer



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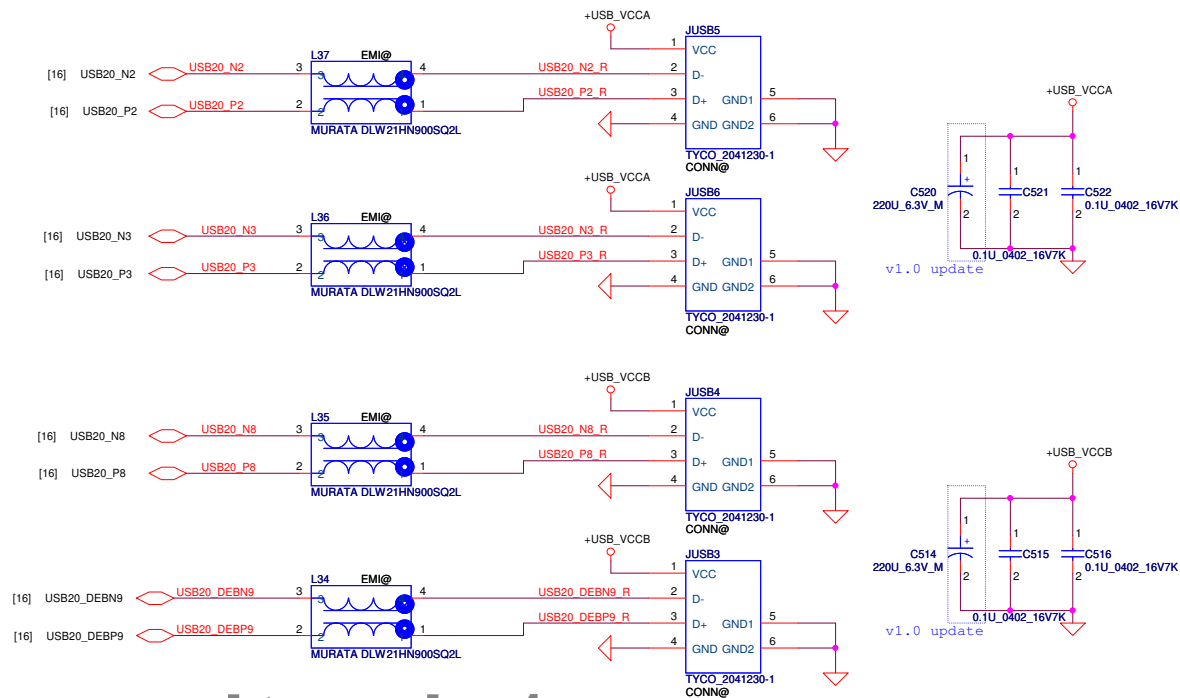
## Charge USB Port



Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPIOA07(pin104)	GPIO22(pin41)	GPIOA11(pin108)	GPIO21(pin40)
S0 (CDP)	1	1	1	1
S3 (SDP)	1	1	1	1
S4/S5 (DCP)	0	0	1	1

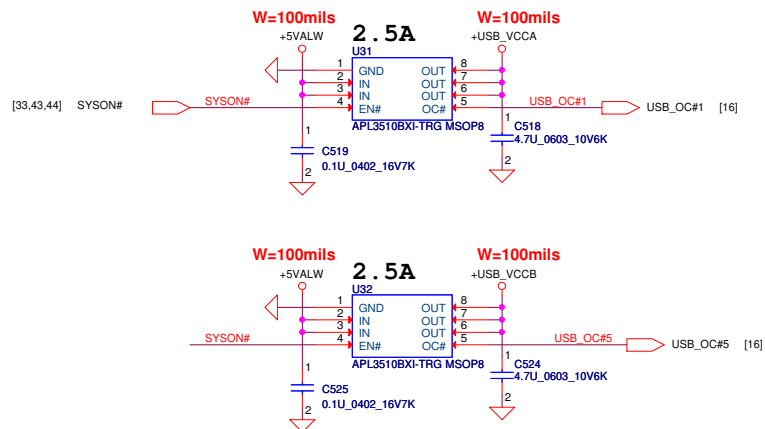
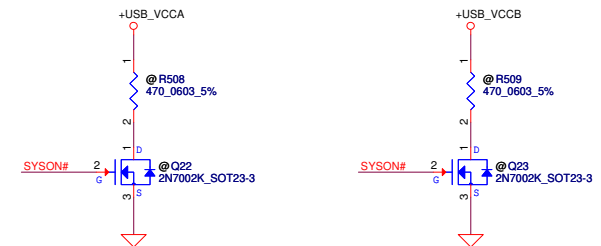
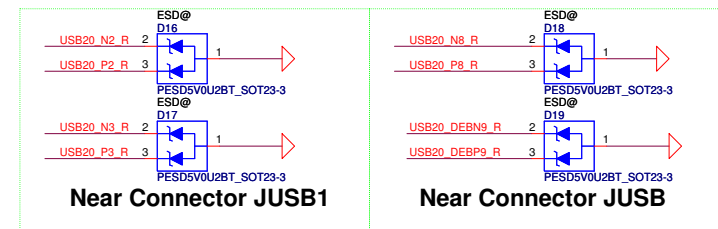
System Global Power State	TPS2546/TPS2544 Mode	Charging	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP		1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs		1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake		0	0	1	1	ILIM_HI

# USB20



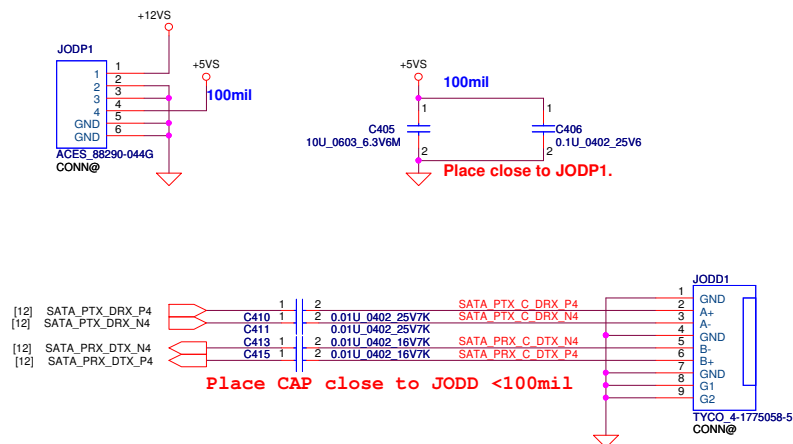
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For USB2.0 ESD diode

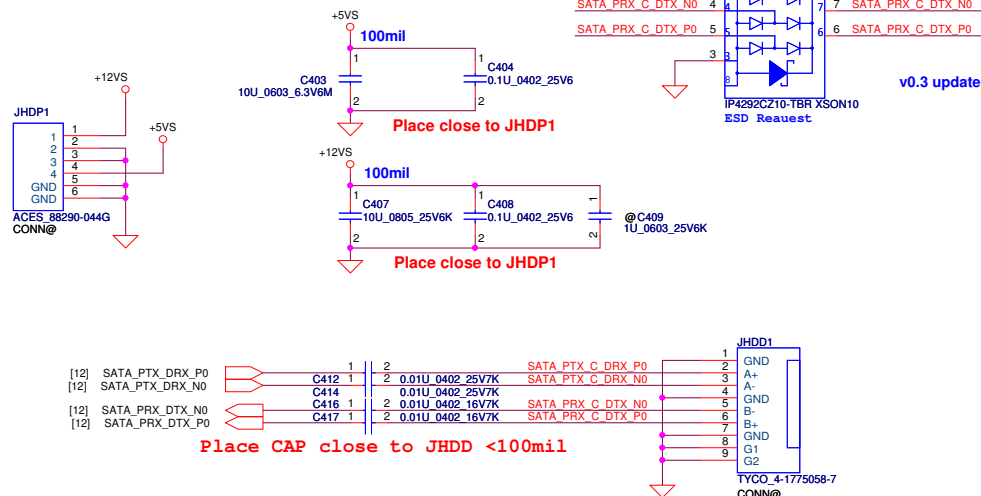


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Size	Document Number	Rev		
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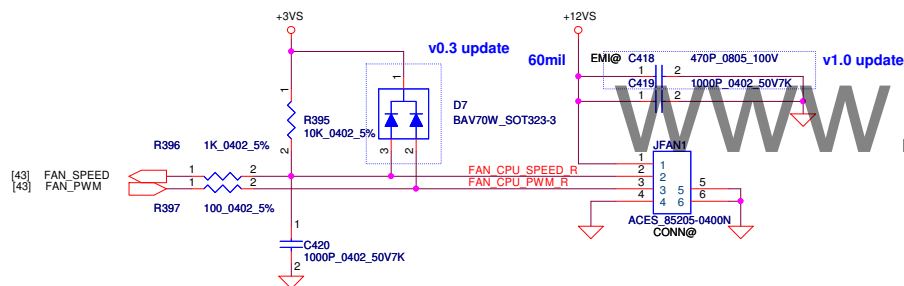
## SATA ODD Conn



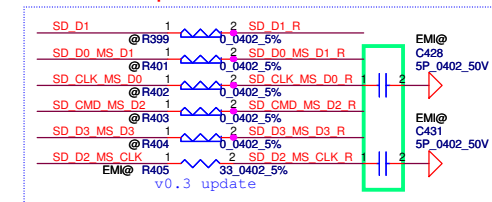
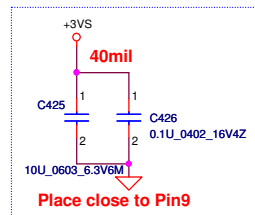
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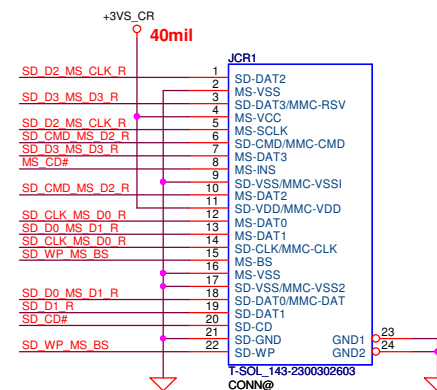
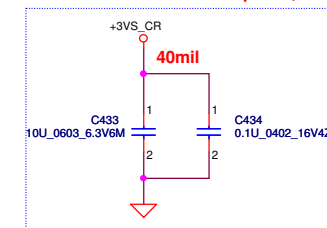
## FAN Control Circuit



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				Date:	Tuesday, September 24, 2013	Sheet 35 of 59

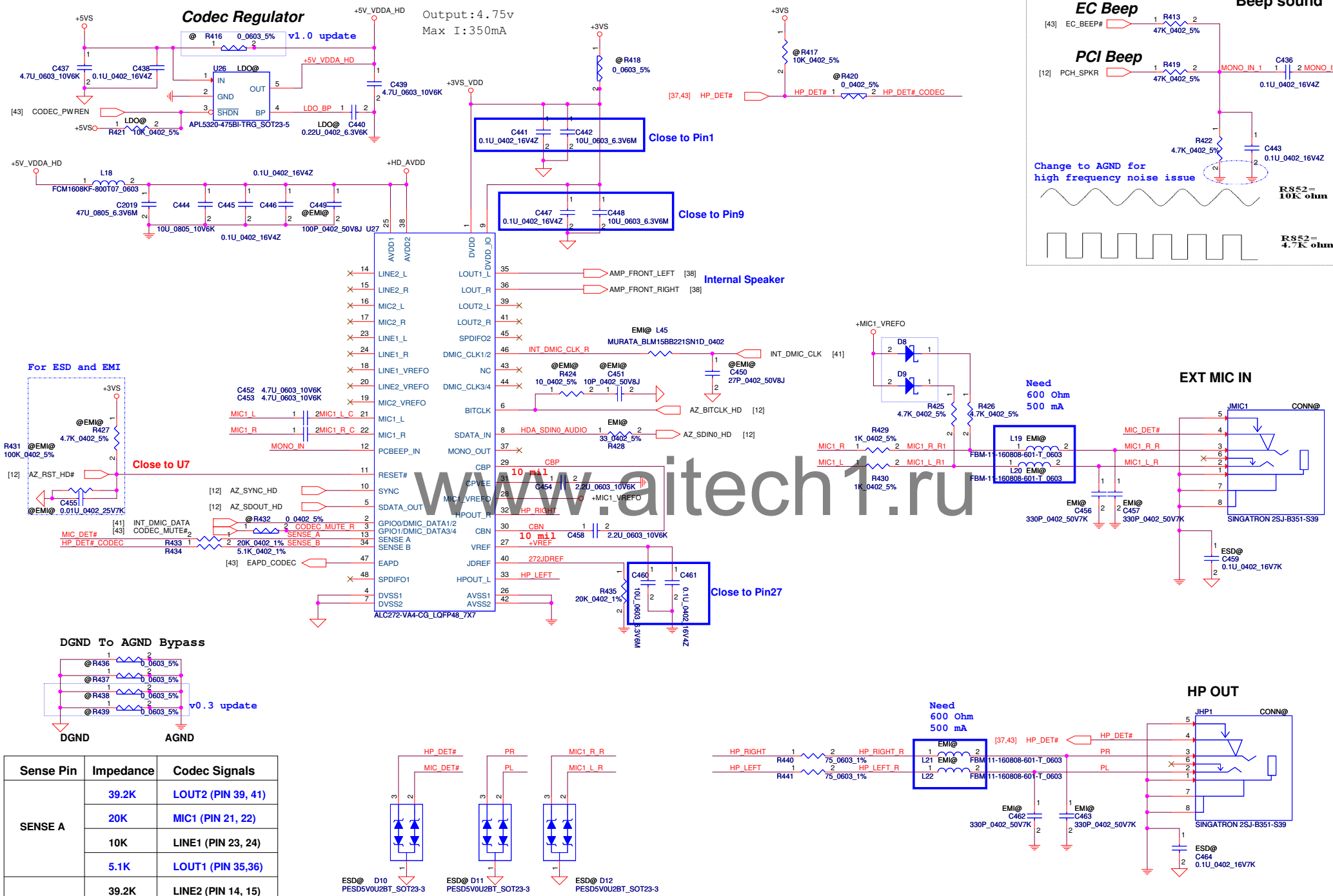


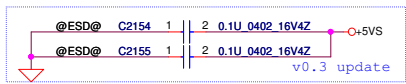
**Place close to JCR1 pin 12,21**



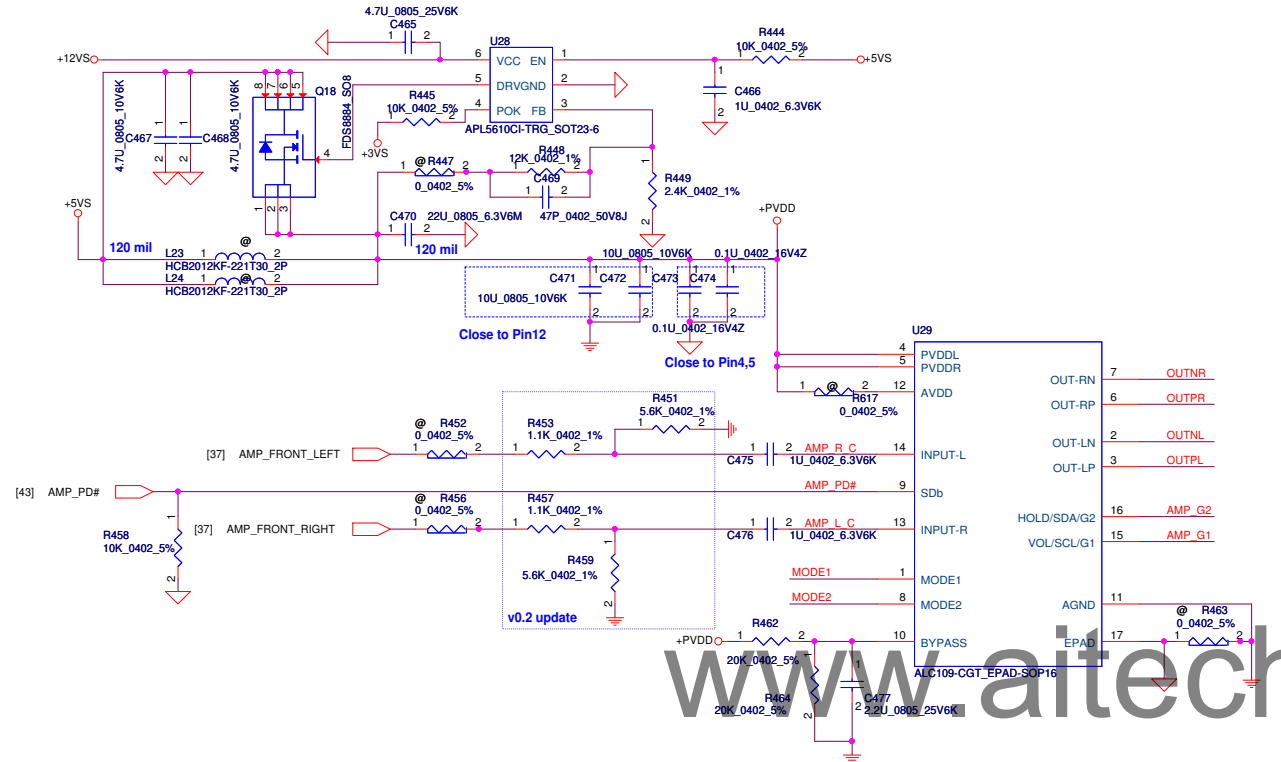
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>RTS5229 Media Card Controller</b>	
Issued Date	2013/04/01	Deciphered Date	2014/04/01	Title	
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				Custom	<b>ZEAO0 LA-A061P M/B</b> Rev 0.3
				Date	Tuesday, September 24, 2013 15:00 36 of 50



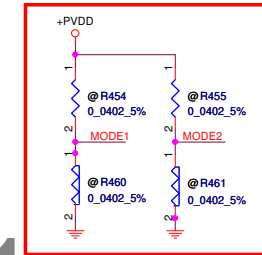




$V_o = 0.8 (1 + R_{606} / R_{607})$   
Output: 4.8V  
Max I: 7.5A

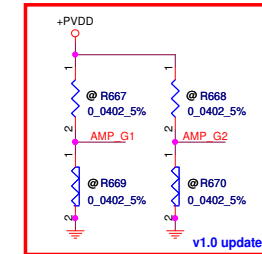


Mode selet: Fix Gain



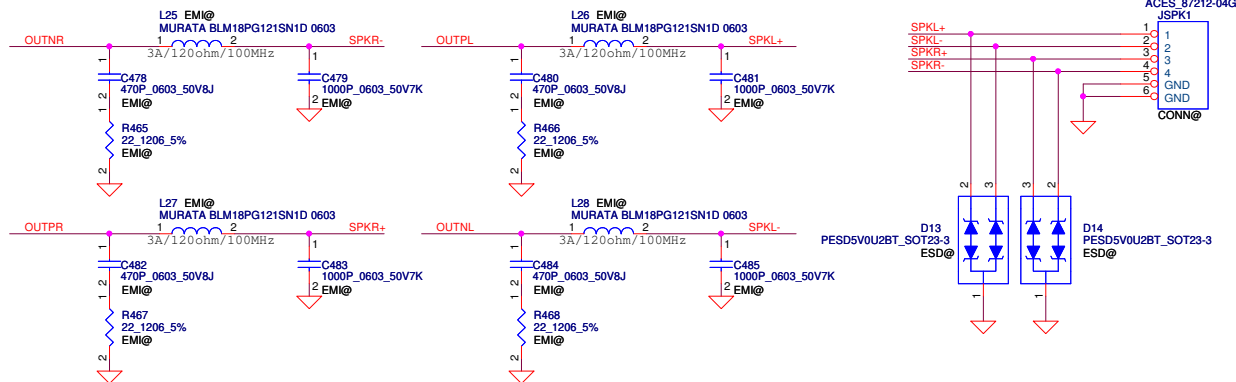
Model1	Model2	Option	Pin15	Pin16
0	0	Fixed Gain	G1	G2
0	1	I2C	SCL	SDA
1	0	PWM	PWM	Hold
1	1	DC	DC	Hold

Gain Select



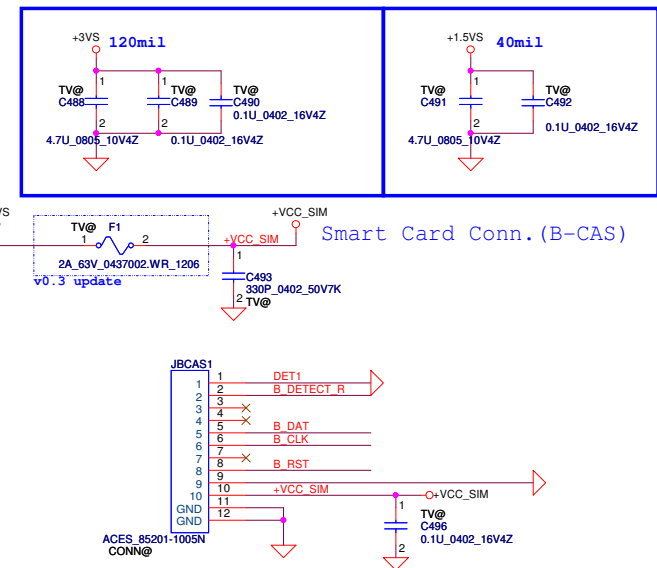
AMP_G1	AMP_G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

(Default)

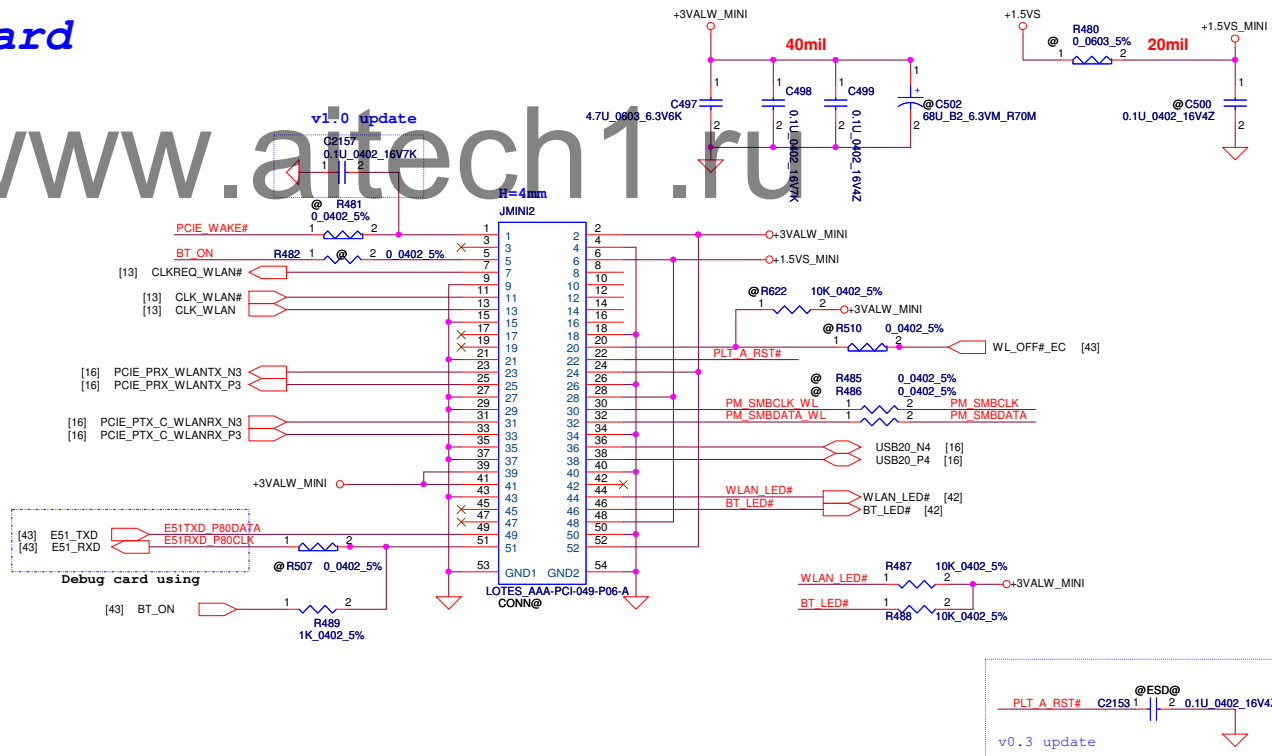
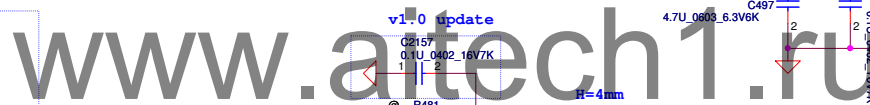




Mini Card Slot 1---TV tuner Current: +3VS : 2750mA, 1.5V: 500mA

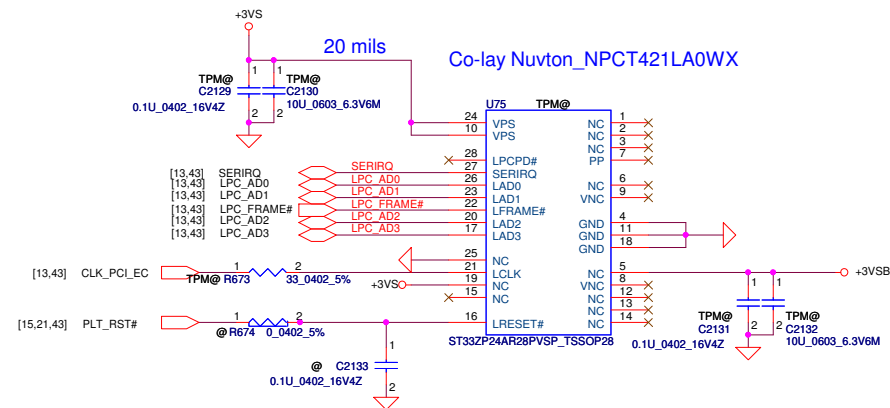


**Mini Card Slot 2--- WLAN Current: 3.3 : 750mA,**

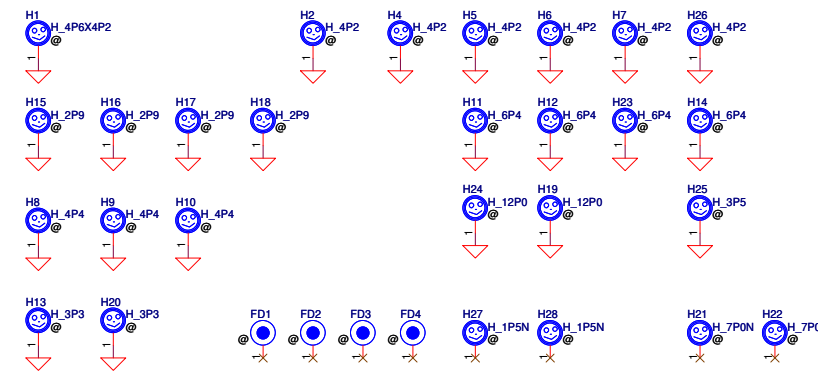


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				Size	Document Number	Rev
				ZEA00 LA-A061P M/B		
Date:				Tuesday, September 24, 2013	Sheet	40 of 59

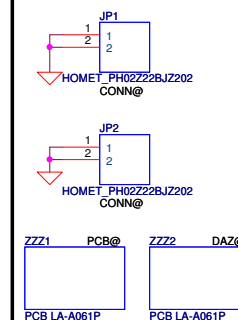
## TPM (Reserve)



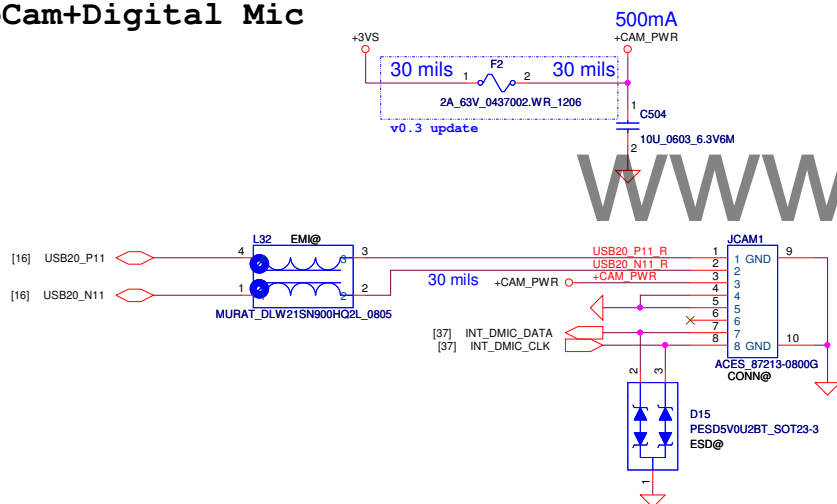
## Screw Hole



## PCH heat sink

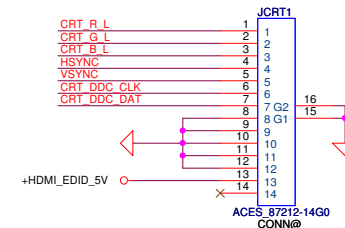
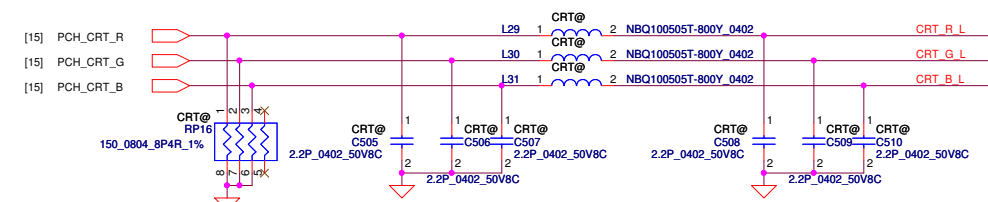


## WebCam+Digital Mic

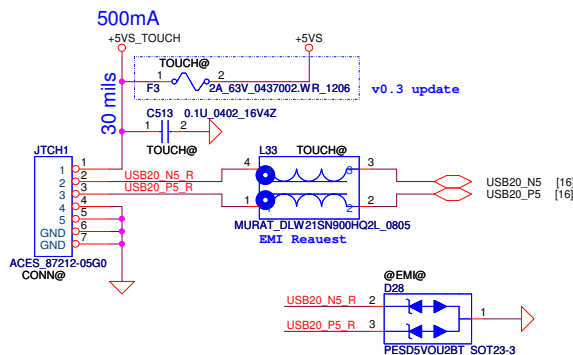


Need PU/PL on PCH/PCH side  
(2.2K\*2pcs for DDC & 150\_8P4R\*1pcs for RGB)

## CRT Conn(Reserve 15pin)



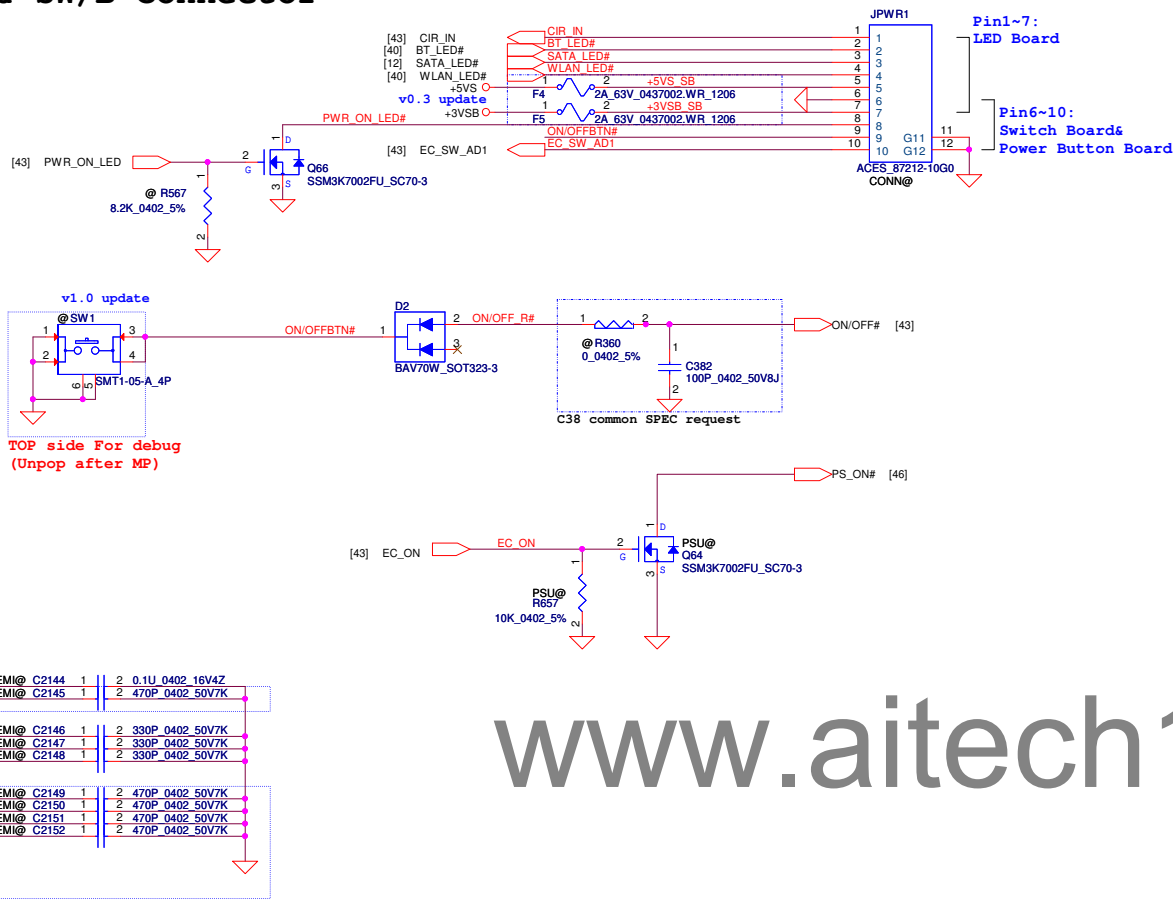
## Touch



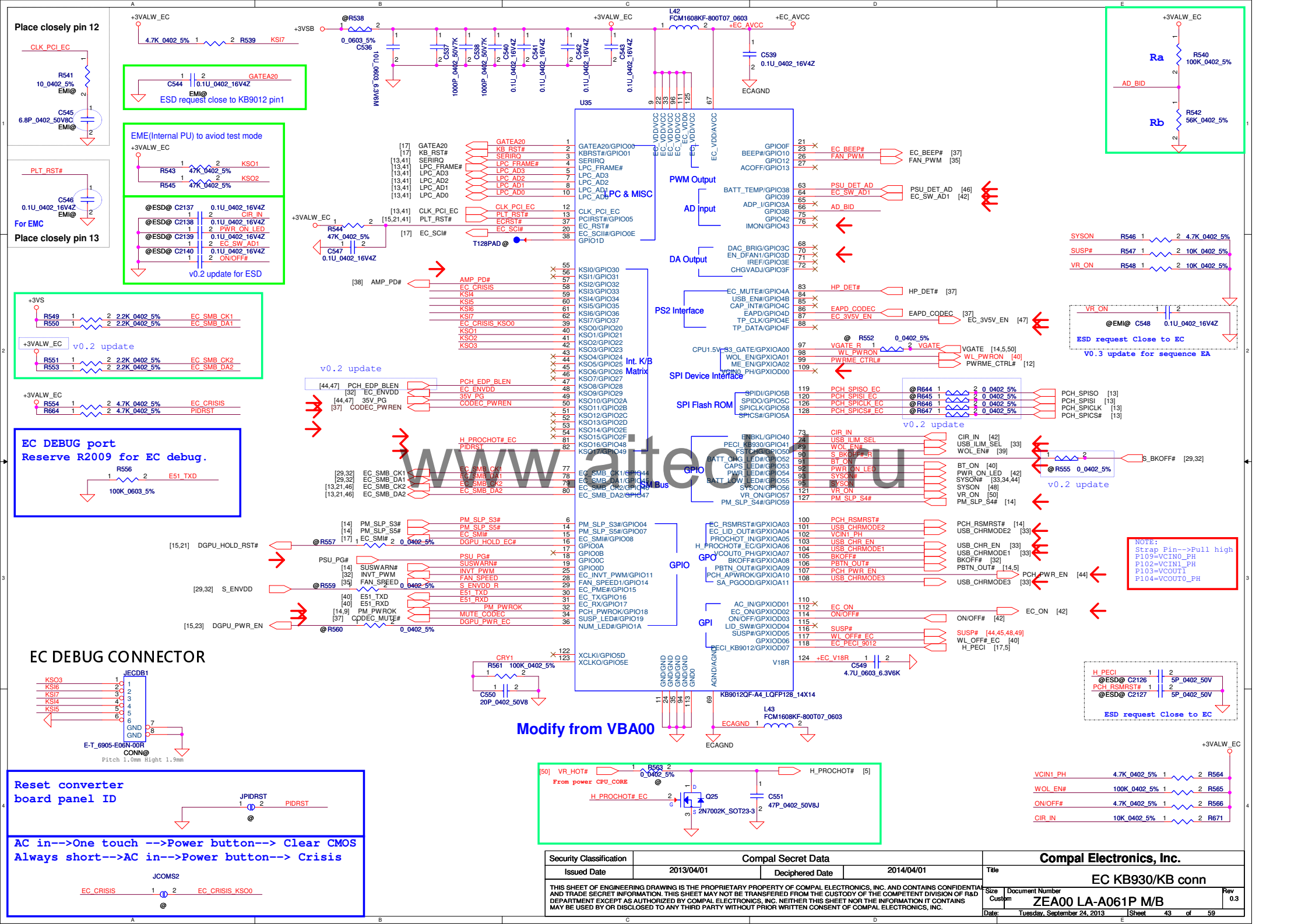
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				ZEA00 LA-A061P M/B	
				Date:	Tuesday, September 24, 2013
				Sheet	41 of 59

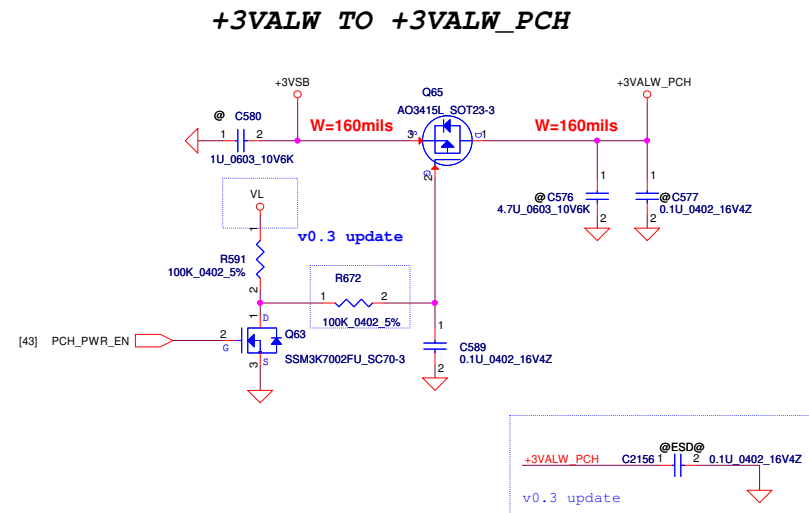
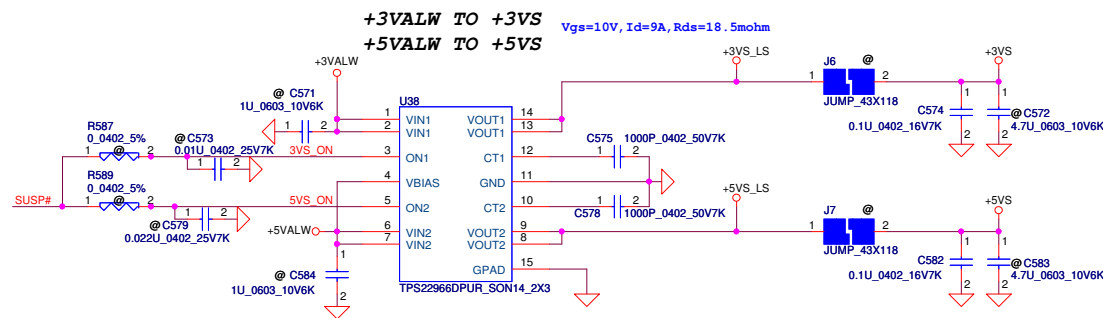
Power/B & SW/B Connector

8Pin sub-board Connecetor

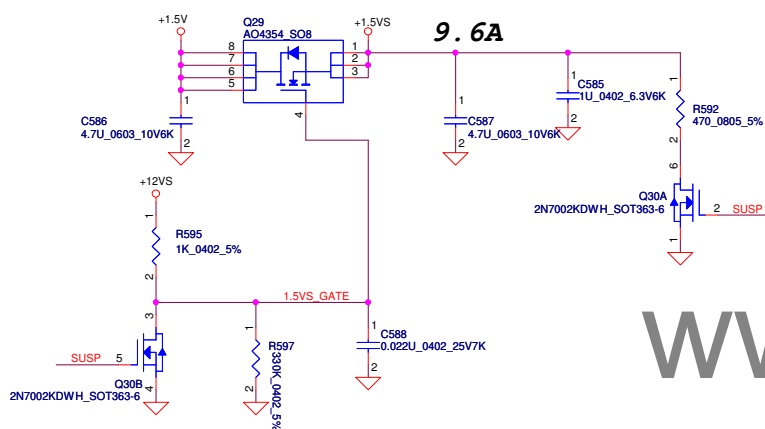




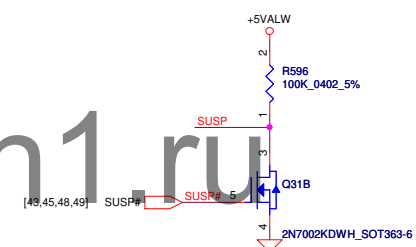




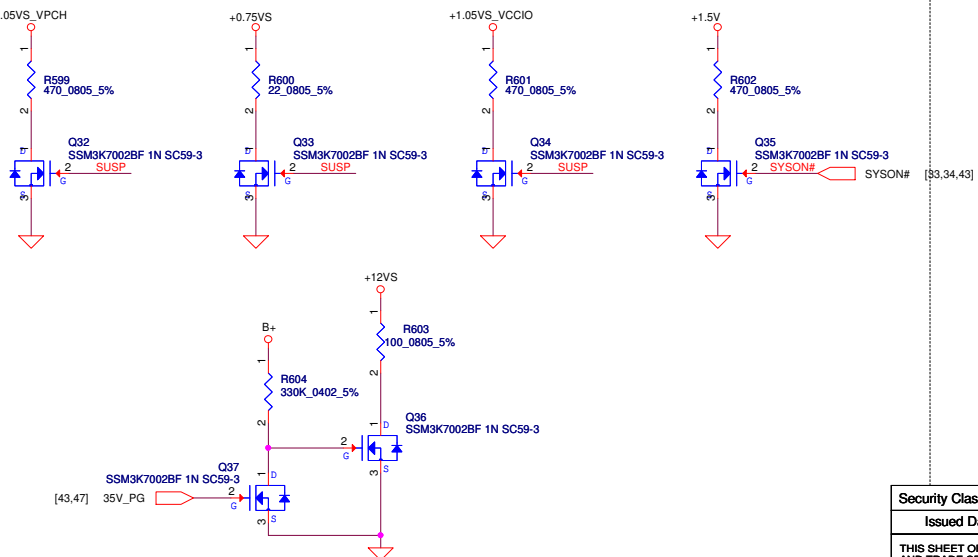
# +1.5V to +1.5VS



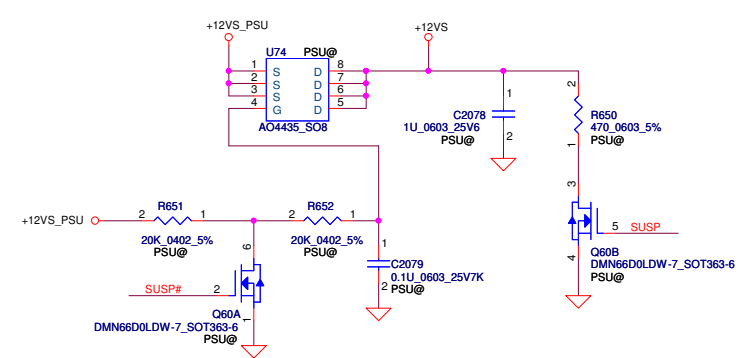
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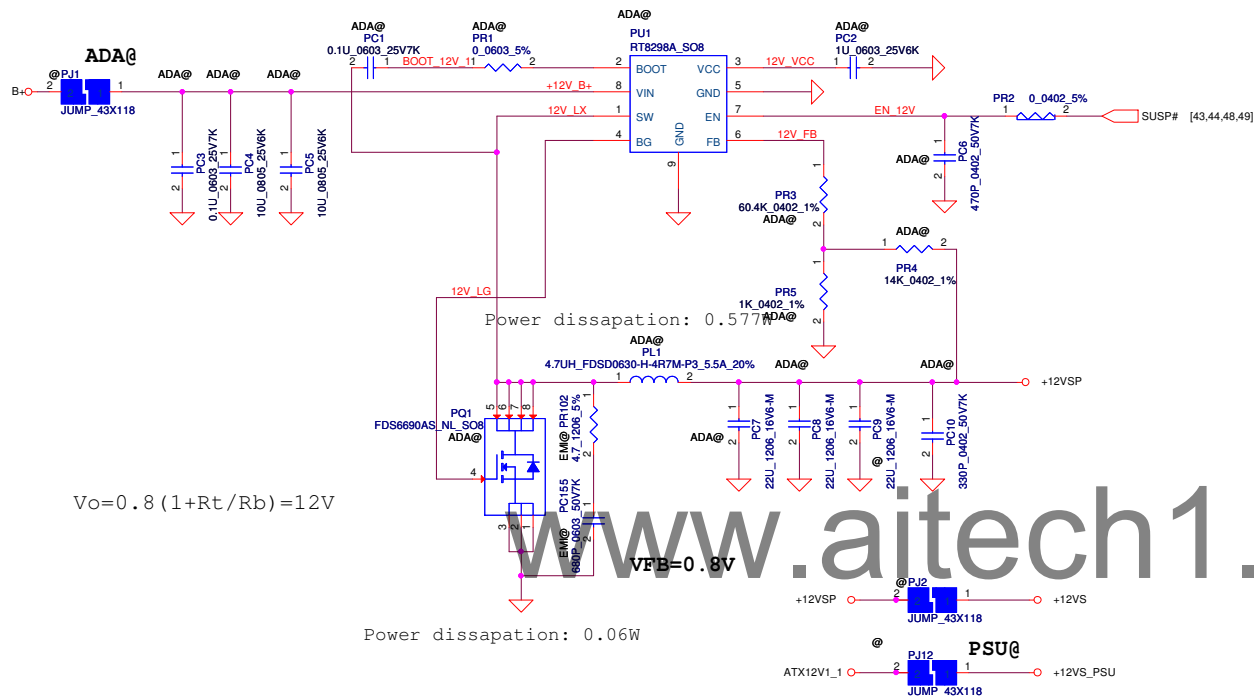
# Discharge circuit



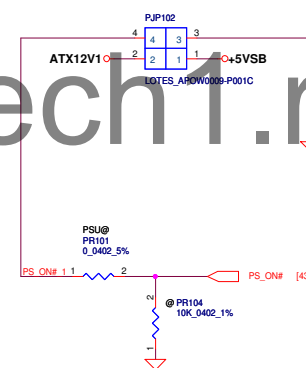
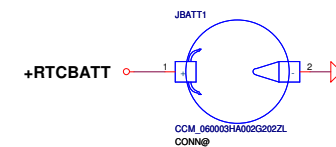
# +12V1 TO +12VS (Reserve for PSU)



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				Size	Document Number
					ZEA00 LA-A061P M/B
				Rev	0.3
				Date	Tuesday, September 24, 2013
				Sheet	44 of 59

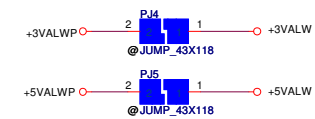


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/04/27				Title			
				Deciphered Date				PWR- 12VSP			
								Document Number			
								VB111 LA-A111 M/B			
								Date: Tuesday, September 24, 2013			
								Sheet 45 of 56			



```
Ventura for CPU side
slave address : 1000001
please placemnet near R-sense
```

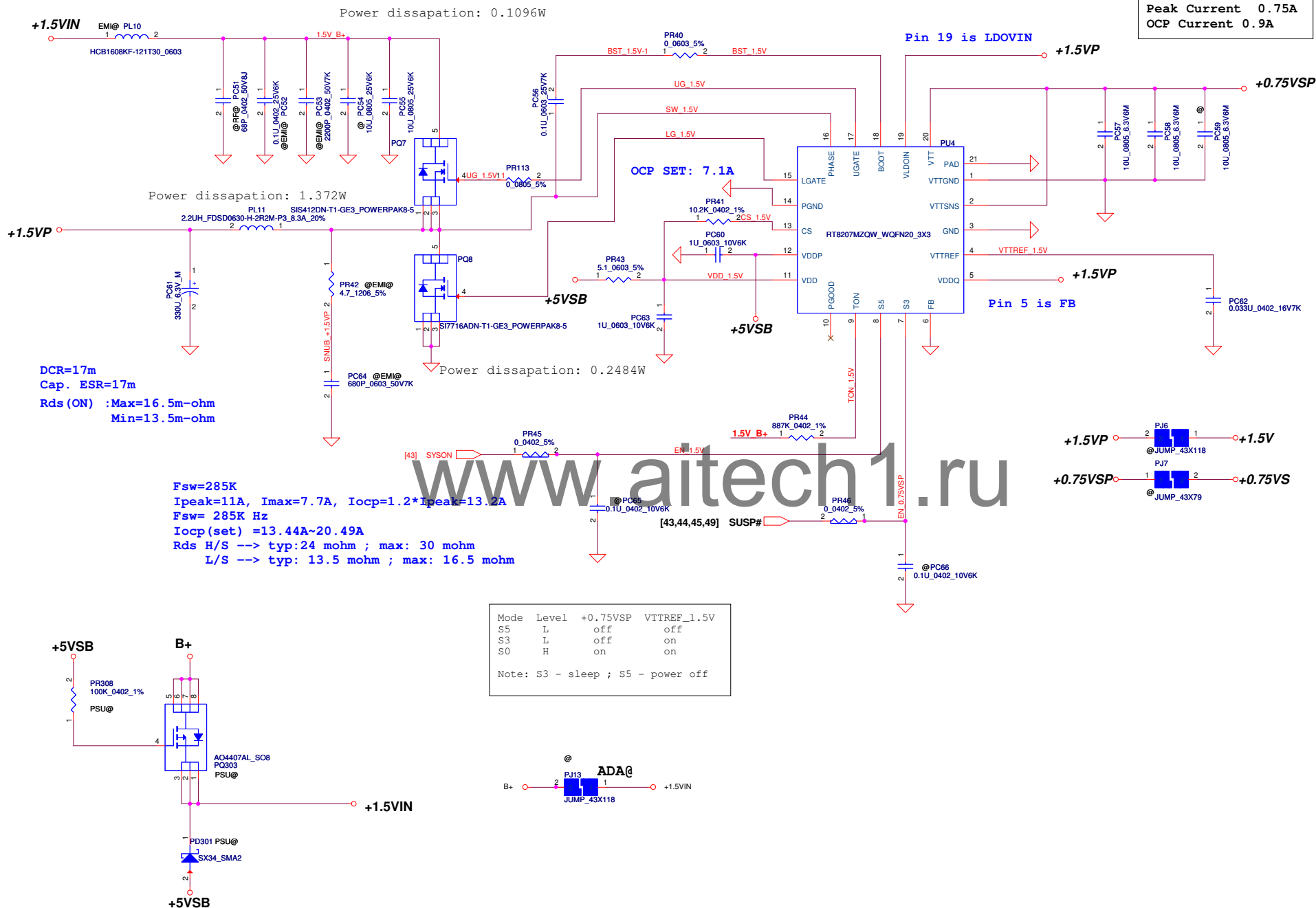
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/01	Deciphered Date	2012/11/12	Title	PSU IN
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Date: Tuesday, September 24, 2013				Sheet	46 of 56



TON (1) SMPS1=300KHZ (+5VALWP)  
(2) SMPS2=300KHZ (+3VALWP)

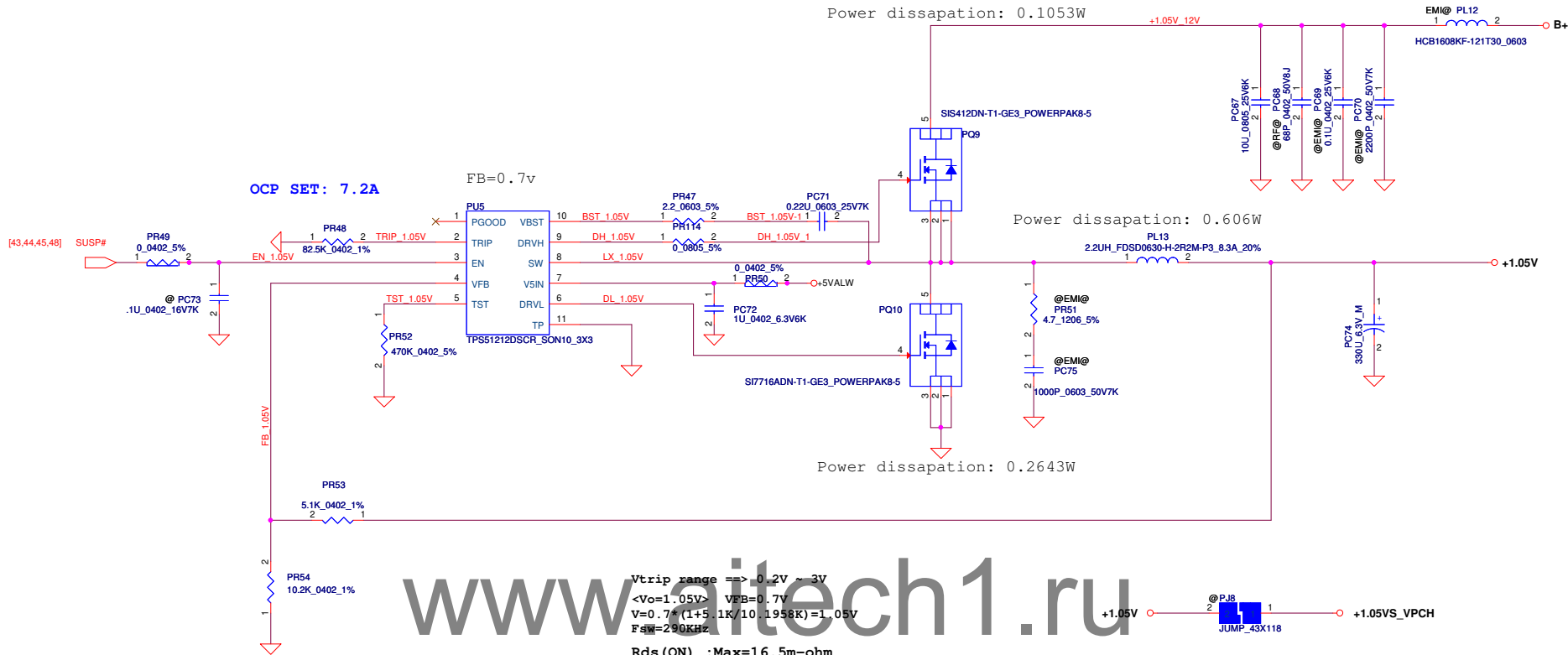
```
+V_3.3VP
Ipeak=4.437A ; 1.2Ipeak=5.325A; Imax=3.106A
Fsw=300K
Iocp>=5.33A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm
```

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR- 3VALWP/5VALWP</b>	
Issued Date	2012/09/01	Deciphered Date	2013/12/31	Title	
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				Document Number	VCA00 LA-9792P M/B
Date:				Tuesday, September 24, 2013	Sheet 47 of 56



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				1.5VP	0.1
				Date: Tuesday, September 24, 2013	Sheet 48 of 56

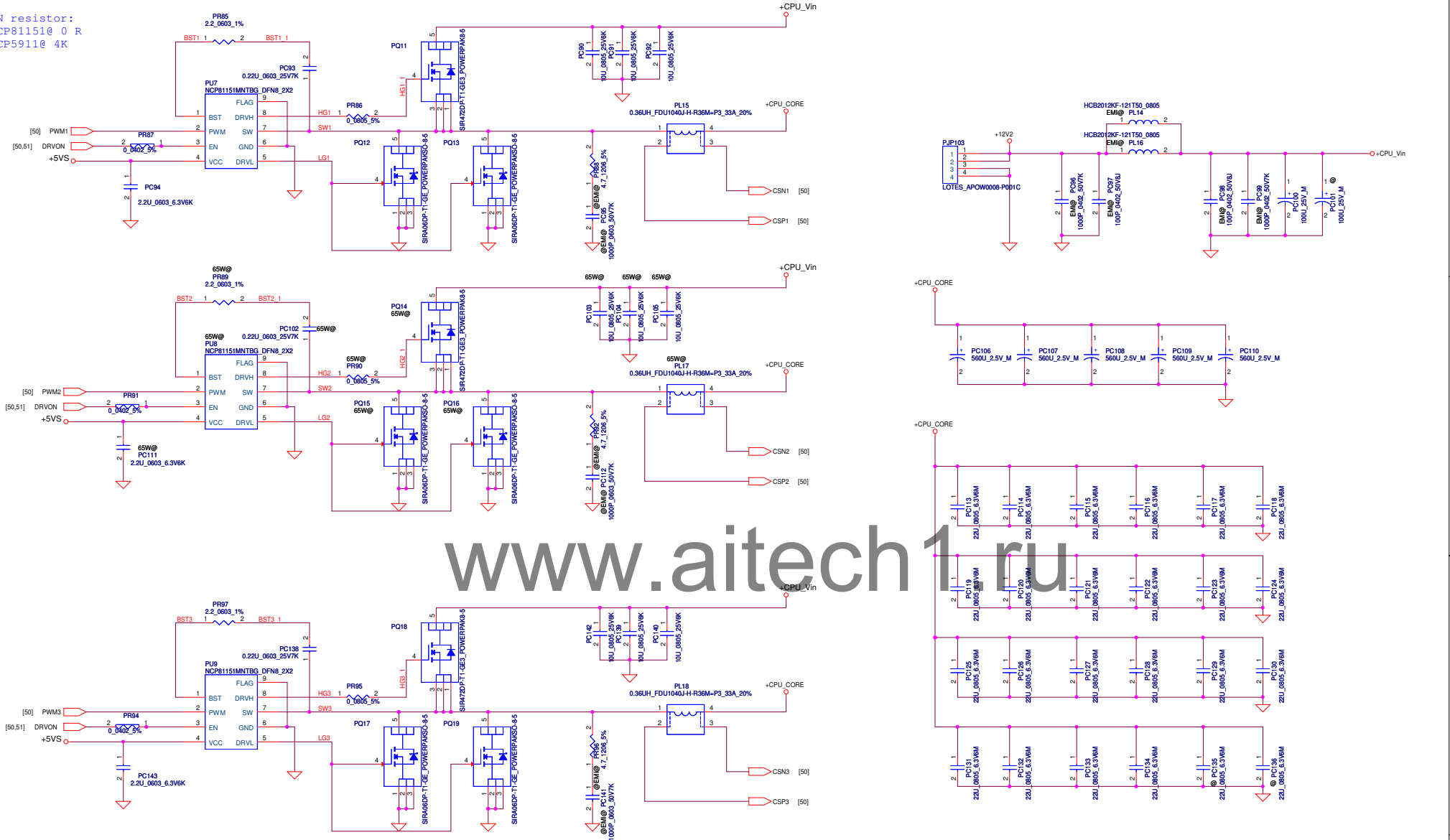




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Issued Date	2012/09/01	Deciphered Date	2013/12/31	Title	+1.05VSP
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				Date	Tuesday, September 24, 2013
				Sheet	49 of 56



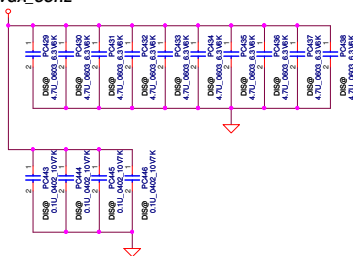
EN resistor:  
NCP81151@ 0 R  
NCP5911@ 4K



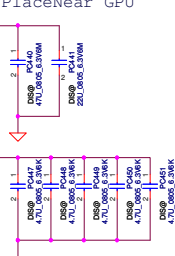
Design for  
N14M-GE2

Follow GB4-128 demand

+VGA\_CORE Place Under GPU



+VGA\_CORE PlaceNear GPU

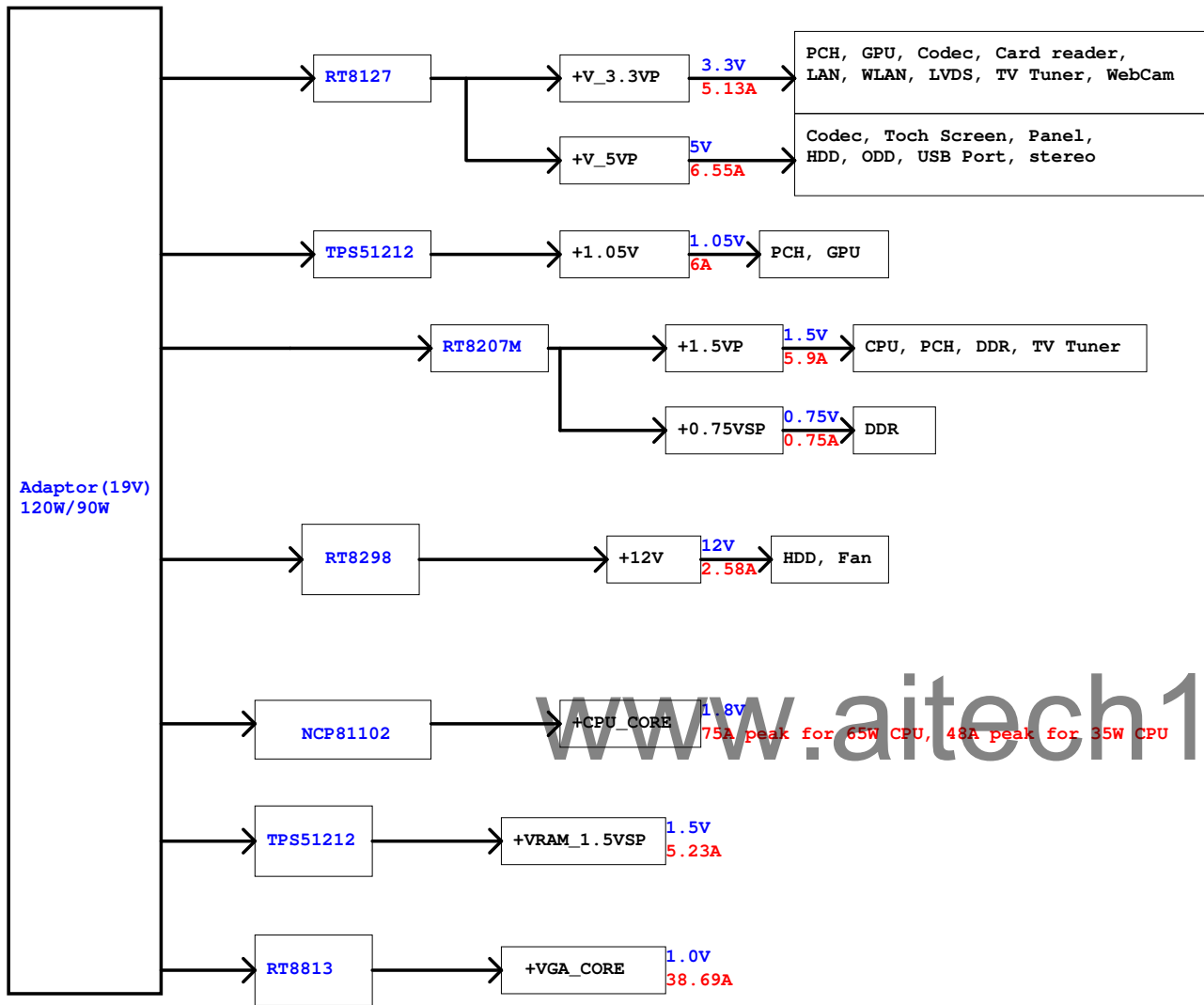


PH701 close to MOSFET  
Trigger point 110 degree

N14P-GE2  
Ipeak=  
Imax=  
Iocp=

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/14	Deciphered Date	2013/12/31	Title	PWR_VGA_CORE/VGA_PCIE
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				Date	Tripoli
				Version	September 24, 2013
				Sheet	52 of 56
				Rev	0.1

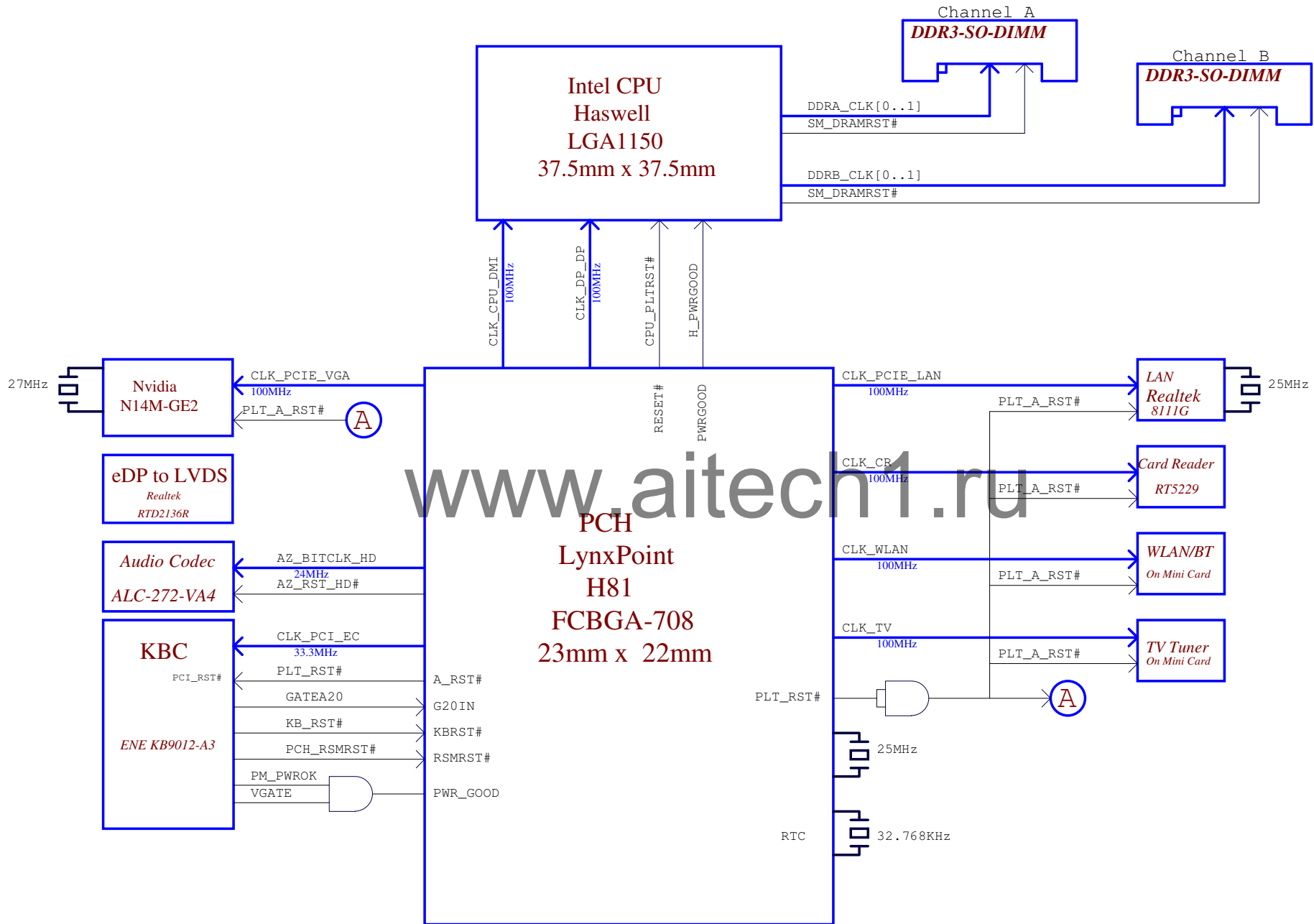




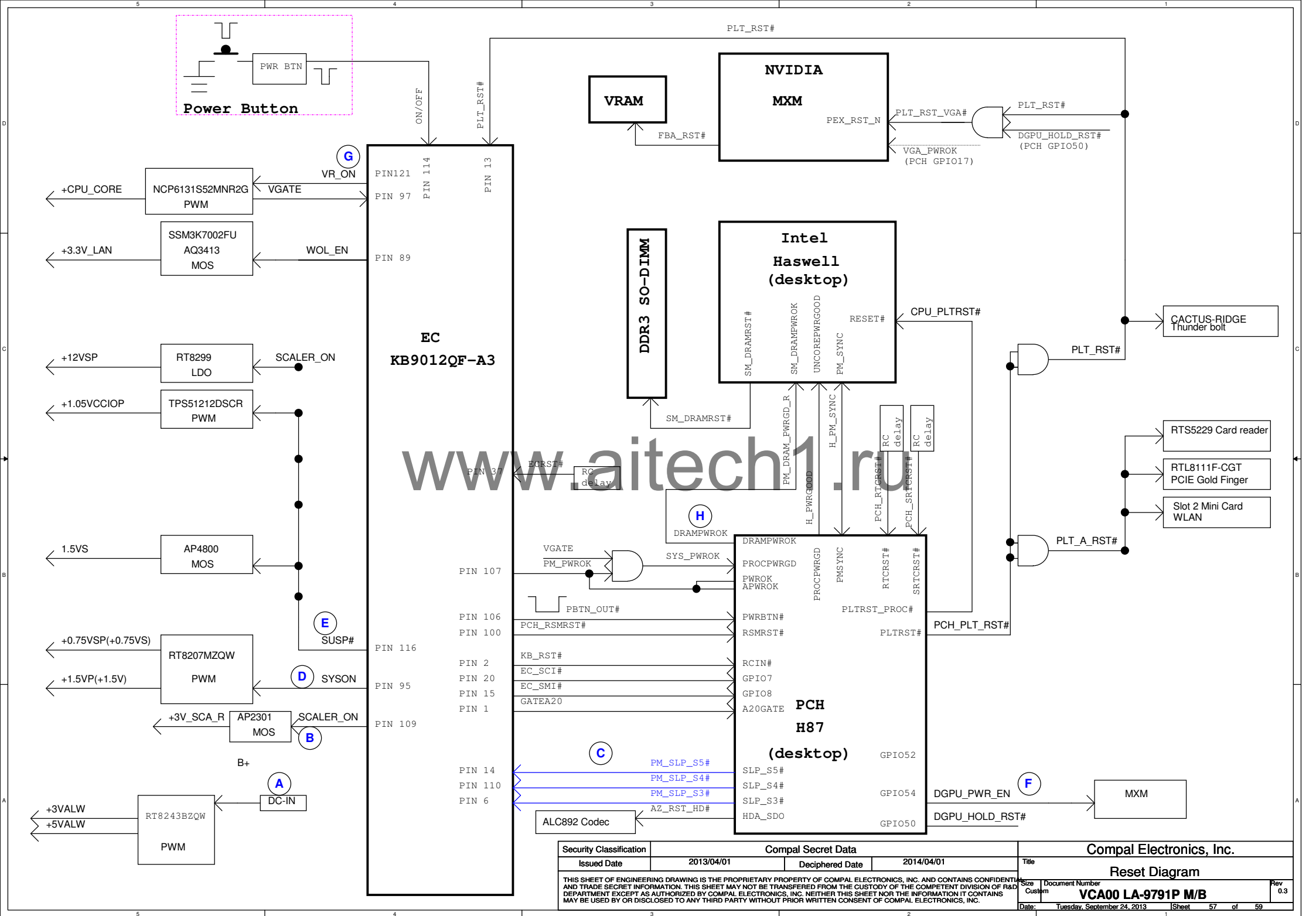
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/09/12	Deciphered Date	2012/09/12	Title	Power Rail
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				Date: Tuesday, September 24, 2013	Sheet 55 of 59



# Clock and Reset Diagram



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Issued Date	2013/04/01	Deciphered Date	2014/04/01	Title
				Clock/Reset Diagram
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Date: Tuesday, September 24, 2013				Sheet 56 of 59



NO		DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	20130604	P47	Add PC154 and Change the pu101 to SA00005A800		For Pericom issue
2.	20130729	P45	Add PR105 ,PC155 Shaber		For ENI Request
3.	20130729	P45	Add PR1		For ENI Request
3.	20130729	P45	Add PR39		For S5 power loss issue

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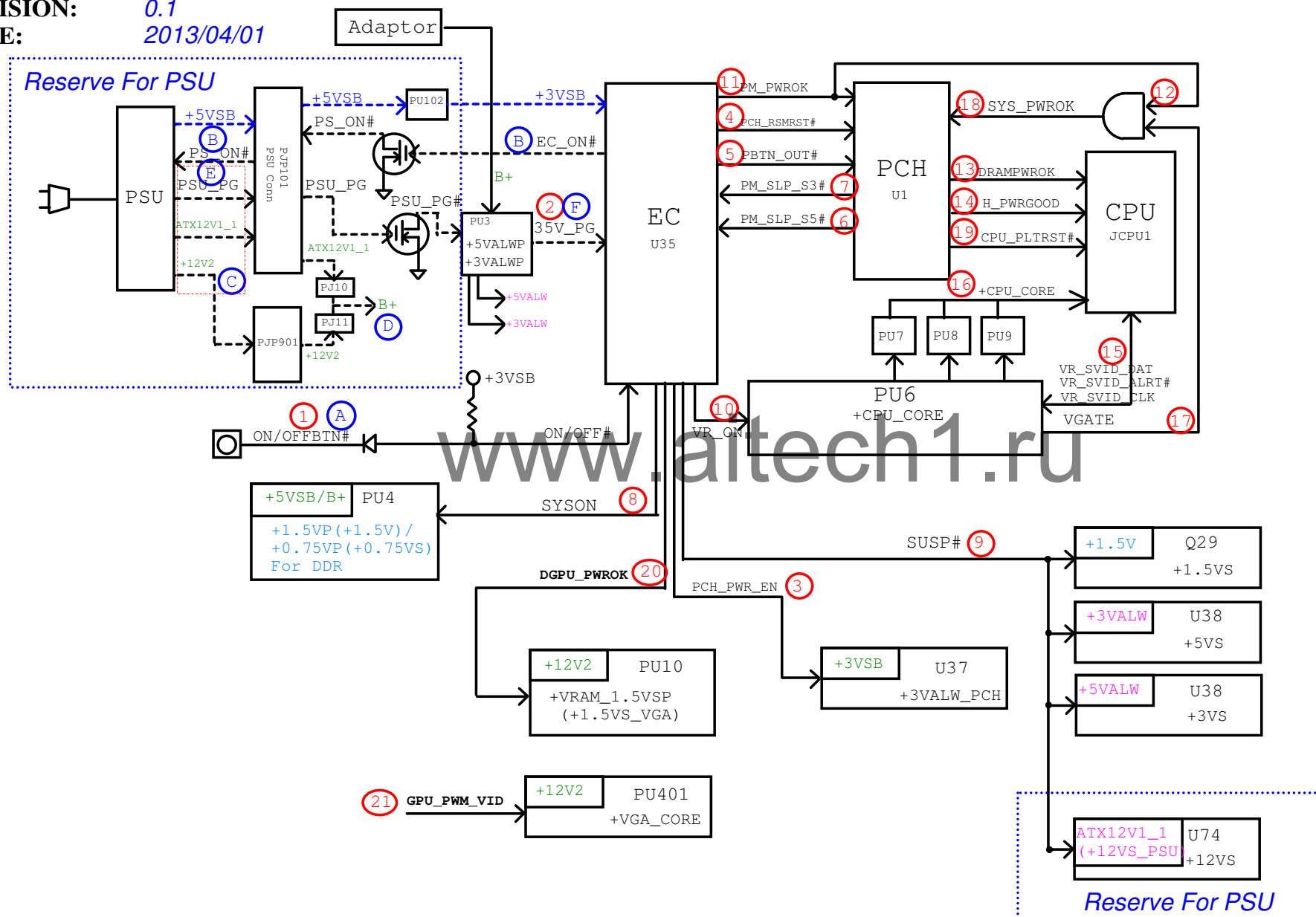
**COMPAL CONFIDENTIAL**

**MODEL NAME:** *ZEA00 Power Sequence Block Diagram (Discrete)*

PCB NAME: LA-A061P

**REVISION:** 0.1

**DATE:** 2013/04/01



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Issued Date	2013/04/01	Deciphered Date	2014/04/01	Title	Power Sequence Diagram
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				Document Number	0.3
CUSTOMER: ZEA00 LA-A061P M/B				Date:	Tuesday, September 24, 2013
				Sheet	58 of 59

HW PIR (Product Improve Record)

ZEA00 LA-A061P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 --> 0.2

GERBER-OUT DATE: 2013/06/20

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
-----				
1.			Change C45 from SF000002V00 to SF000003X00	
2.			Change +LCDVDD enable control from EC to LVDS convertor,un-pop R367 and R365 change short pad.	
3.			<del>Change LCD_BACKLIGHT control from EC to LVDS convertor,un-pop R364 and R363 change 0 ohm.</del>	
4.			Remove un-used components(U18,R335,R336,C357,C359,C360,R338,R339) for eDP to LVDS convertor.	
5.			Pop R428 for AZ_SDIN0_HD.	
6.			U2 footprint change from socket to IC.	
7.			Add RH11	
8.			Change Y2 from SJ10000CU00 to SJ10000DE00,change C106 & C107 from 27pF to 4.7pF	
9.			Change R423 location to L45	
10.			Change D7 from SC2N202U010 to SC600000B00 for 替代料	
11.			Change Q29 from SB548000210 to SB000002N00.	
12.			Change D8&D9 from SCS00002G00 to SCS00000Z00	
13.			X1 code change:1.Change Q2,Q3,Q4,Q5,Q30,Q31 from SB01000JE00 to SB00000E000. 2.Change Q9 from SB934130020 to SB934130000. 3.Change Q10 from SB00000FC00 to SB00000F400. 4.Change L1 from SM01000JE00 to SB01000JN00.	
14.			Change R551 & R553 pull-high from +3VS to +3VALW_PCH for leakage.	
15.			Add R677 & R678 & R679 for PTC request, Change R473,R490,R679,R677,R678 from 0ohm to PTC(SP040005X00).	
16.			Change Q10 from SB00000FC00 to SB00000L800 for 替代料	
17.			Remove R469 0ohm for TV.	
18.			Add C2134 ,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2143 for ESD.	
19.			Remove JXDP1,OC1,OC2,RC3,RC4,R125,R126.	
20.			Pop U7&R231, un-pop R228 for PLT_RST_VGA#.	
21.			Swap SATA_PRX_DTX_N1 & SATA_PRX_DTX_P1 for m-SATA pin define.	
22.			Un-pop LAN power components Q26,Q27,R573,R574,C562.	
23.			0 ohm change to short pad: R347,R585,R507,R674,R644,R645,R646,R647	
24.			Change R453&R457 from 0ohm to 1.1K, R451&R459 from 300ohm to 5.6Kohm.	
25.			Pop R438,R439 for ESD request.	

PVT change list:  
1. Change Q10 from SB00000FC00(EOL soon) to SB000002N00(同Q29),SB00000FC00 as 2nd source.Schematic,需驗證

2. Change U23 pin12\_+USB3\_VCCA to +USB3\_VCCB, pop U22, un-pop U24 for USB charger
3. R365 change from short pad to 0ohm.
4. U5 pin5 change from +3VSto +3VALW\_PCH for BCM43142 wake from WLAN issue.
5. Change R473,R490,R677,R678,R679 from SP040005X00\_0603 size to F1,F2,F4,F5,F3 SP040003S00\_1206 size.
6. Change L11 from SM010014520 to SM01000EJ00 for ACL request
7. Change L8 from SM010007W00 to SM010019400 for ACL request
8. Change D7 from SC2N202U010 to SC600000B00(same as D1/D2), SC2N202U010 as 2nd source..
9. Change RP19 from SD309510A80(T88 P/N) to SD309510A10.
11. Change R276 from 10k to 100k for +3VS\_VGA rise time.
12. Change R672 from 10k to 100k for +3VALW\_PCH rise time.
14. Change R438 & R439 from 0\_0603 to short pad.
15. Un-pop C125 & C548 for sequence EA.
16. Change C394, C398,C520 & C514 from 220uF(LELON\_SF000001F00) to 100uF (Panasonic\_SF000005100) to meet Inrush EA & ACL request.
17. Change C170 & C171 from 12pF to 10pF for EA.
20. Change C106 & C107 from 4.7pF to 10pF for 25MHz crystal.
21. Add R677 & reserve R678 on U5 AND gate for PLT\_A\_RST#
13. Change JUSB1 & JUSB2 from DC23300AE00 to DC233008R00(VBA11)
24. Change R591 pull-high from +5VSB to VL for power S5 Erp request.
22. Change D20 & D21 from SC300001Y00 to SC300002F00 for ESD request
23. Change D22 & D23 from SCA00001100 to SCA00000T00 for ESD ACL request
10. Add C2144-C2152 for EMI request.
18. Change R402 from short pad to 22ohm for EMI, R399,R401,R403 & R404 change from short pad to 0 ohm for EMI request.
19. Reserve C2153,C2154,C2155,C2156, add D29 for ESD.
20. Change R282 from 100k to 2k, R277 from 470 to 22 ohm for GPU power sequence.
21. Change Y1 from SJ100001K00 to SJ10000FA00 ,C102 & C107 to 6pF.

- pre-MP change list:
1. Change R399,R401,R402,R403,R404 from 0ohm to short pad.
2. Add C2157 and reserve C2158.
3. Change R8,R470,R669,R670,R416 from 0ohm to short pad.
4. Un-pop JECDB1 & SW1.
5. For R3 P/N, change PCH P/N from SA00006RF00 to SA00006RF20, PCB P/N from DA60011S000 to DA60011S010 and GPU P/N from SA00006ZF00 to SA00006ZF10.
6. Change C520 & C514 from 100uF to 220uF.
7. Pop C2149~C2152 for ESD request.
8. Change C559 & C2128 from 0603 to 0805.
9. Change C2145 from 0.1uF to 470pF, change C2149~C2152 from 330pF to 470pF for EMI.
10. Add C418 for EMI.

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Issued Date	2013/04/01	Deciphered Date	2014/04/01	Title		
				HW-PIR		
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